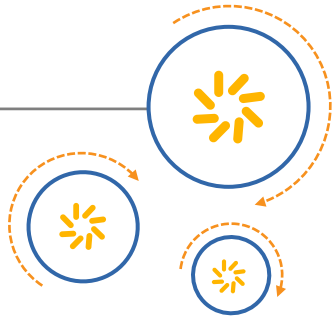
Qualcomm Technologies, Inc.



Qualcomm® Snapdragon™ 600 Processor APQ8064

Data Sheet

February 2016

Qualcomm Technologies, Inc.
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LM80-P0598-1 Rev. B

Revision history

Revision	Date	Description
A	June 1, 2015	Initial Release
B	February 10, 2016	Removed Figure 3.1 and Section 3.1.1

Contents

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1 Introduction

This document describes features and functionality of Qualcomm® Snapdragon™ 600 processors (model APQ8064) for embedded computing.

Qualcomm processors for embedded computing are dedicated to support embedded device OEMs in several ways:

- Longevity beyond lifecycle of mobile chipsets through 2020
- Detailed documentation for developers
- Availability of development kits/community board for early access
- Multiple OS support including mainline Linux support
- Availability of several computing module partners for customization for your individual projects/products

Snapdragon 600 processors deliver high-performance computing, low-power consumption, and a rich multimedia experience for embedded devices.

It is an ideal solution for any application that requires computing horsepower and integrated Wi-Fi/Bluetooth connectivity, such as Smart Home, Industrial Appliances, Digital Media and TV dongles, Smart Surveillance and Robotics.

Snapdragon supports a clear deployment path for embedded device OEMs and developers – starting with single-board computers and development kits, and scaling up to customer solutions, integration services, and production-ready, customizable computing modules.

For further information, visit
https://www.qualcomm.com/products/snapdragon/embedded-computing.

1.1 Documentation overview

This document is the data sheet for the APQ8064 28 nm CMOS fabrication, including:

- RF transceiver
  - WGR7640 IC for GPS
- Power management: PMM8920 IC
- WLAN and FM radio: QCA6234 IC
- Audio codec: WCD9311 IC

1.2 Terms and acronyms

Table 1-1 defines terms and acronyms that may be used throughout this document.Special marks

Table 1-1 Terms and acronyms

Term	Definition
A2DP	Advanced audio distribution profile
ADC	Analog-to-digital converter
AES-XTS	Accelerate file system encryption
AFLT	Advanced forward link trilateration
APQ	QUALCOMM application processor
ARM	ARQ response mode
ARQ	Automatic repeat request
ARP	Address resolution protocol
AWB	Auto white balance
AXI	Advanced extensible interface
BAM	Business access manager
BER	Bit error rate
bps	Bits per second
BT	Bluetooth®
CCMP	Counter-Mode/CBC-Mac Protocol (IEEE 802.11I encryption algorithm)
CDMA	Code division multiple access
CRCI	Client rate control interfaces
CSI	Camera serial interface
CSIM	cdma2000 Application on UICC. Defined in 3GPP2 TSG-C specification C.S0065
DAC	Digital-to-analog converter
DDR	Double data rate
DFSD	Design for software debug
DM	Data mover
DRM	Digital rights management
DSI	Display serial interface
DSP	Digital signal processor
EBI	External bus interface
EDR	Enhanced data rate
EGNOS	European geostationary navigation overlay system
ETM	Embedded trace macrocell
GLONASS	Global orbiting navigation satellite system
GNSS	Global navigation satellite system
GPGPU	General purpose computing on the GPU (graphics processing unit)

Table 1-1 Terms and acronyms (Continued)

Term	Definition
GPIO	General-purpose input/output
GPS	Global positioning system
GSBI	General serial bus interface ports
HDCP	High-bandwidth digital content protection
HDMI®[a]	High Definition Multimedia Interface
I^2C	Inter-integrated circuit
I^2S	Inter-IC sound
JPEG	Joint Photographic Experts Group
JTAG	Joint Test Action Group (ANSI/ICEEE Std. 1149.1-1990)
kbps	Kilobits per second
KPSS	Krait processor subsystem
LCC	LPASS clock controller
LCD	Liquid crystal display
LDPC	Low density parity check
LMEM	Local memory
LPA	Low-power audio
LPDDR	Low-power double data rate
LSbit or LSByte	Defines whether the LSB is the least significant bit or least significant byte. All instances of LSB used in this manual are assumed to be LSByte, unless otherwise specified.
LVDS	Low-voltage differential signaling
MCLK	Master clock
MDP	Mobile display processor
MI^2S	Multiple inter-IC sound
MIDI	Musical instrument digital interface
MIPI	Mobile industry processor interface
MIMEM	Multimedia internal memory
ML	Maximum likelihood
MMC	Multimedia card
MRC	Maximum Ratio Combining
MRL	Measurement result list
MSbit or MSByte	Defines whether the MSB is the most significant bit or most significant byte. All instances of MSB used in this manual are assumed to be MSByte, unless otherwise specified.
NFC	Near-field communication
OMA	Open mobile alliance
PA	Power amplifier
PCI	Protocol capability indicator

Table 1-1 Terms and acronyms (Continued)

Term	Definition
PCIe	Protocol capability indicator express
PCM	Pulse coded modulation
PDM	Pulse-density modulation
PM	Power management
PMIC	Power management integrated circuit (with RTC)
QDSP6	Qualcomm digital signal processor, 6th-generation
QFPROM	QUALCOMM fuse programmable read only memory
QGIC	Qualcomm Generic Interrupt Controller
RDS	Radio data system
RBDS	Radio broadcast data system
RGB	Red-green-blue
RPM	Resource power manager
RTT	Round trip time
SATA	Serial ATA
SAW	Surface acoustic wave
SBI	Serial bus interface
SD	Secure digital
SDC	Secure digital controller
SDIO	Secure digital input/output
SDR	Single data rate
SFS	Secure file system
SIM	Subscriber identification module (Smart Card)
SMPL	Sudden momentary power loss
SMPS	Switched-mode power supply
SPI	Serial peripheral interface
sps	Symbols per second (or samples per second)
SPSS	Sensor peripheral subsystem
SSBI	Single-wire SBI
STBC	Space time bock coding
TCXO	Temperature-compensated crystal oscillator
TKIP	Temporal key integrity protocol
TLMM	Top-level mode multiplexer
TSIF	Transport stream interface
TxBF	Transmit Beamforming
UART	Universal asynchronous receiver transmitter
UICC	Universal integrated circuit card

Table 1-1 Terms and acronyms (Continued)

Term	Definition
UIM	User identity module
UMTS	Universal mobile telecommunications system (a 3G initiative)
USB	Universal serial bus
USIM	User services identity module or universal subscription identity module
VCTCXO	Voltage-controlled, temperature-controlled, oscillator
VDD	Video display data from camera firmware
VFE	Video front-end
VPE	Video preprocessing engine
WAAS	Wide-area augmentation system
WAPI	WLAN Authentication and Privacy Infrastructure - a Chinese national standard for wireless LANs
WCD	Wireless connectivity device
WCN	Wireless connectivity network
WEP	Wired equivalent privacy
WGR	Wireless GPS receiver
WLNSP	Wafer-level nano-scale package
WPA	Wi-Fi protected access (IEEE 802.11 wireless networking)
WPS	WLAN protected setup
XO	Crystal oscillator
XPU	External Protection Unit (X - Memory/Register/Address)

a. HDMI, the HDMI Logo, and High-Definition Multimedia Interface are trademarks or registered trademarks of HDMI Licensing LLC in the United States and other countries.

1.3 Special marks

Table 1-2 defines special marks used in this document.

Table 1-2 Special marks

Mark	Definition
[ ]	Brackets ([ ]) sometimes follow a pin, register, or bit name. These brackets enclose a range of numbers. For example, GPIO_INT [7:0] may indicate a range that is 8 bits in length, or DATA[7:0] may refer to all eight DATA pins.
_N	A suffix of *_N* indicates an active low signal. For example, RESIN_N.
0x0000	Hexadecimal numbers are identified with an *x* in the number; for example, 0x0000. All numbers are decimal (base 10) unless otherwise specified. Non-obvious binary numbers have the term binary enclosed in parentheses at the end of the number; for example, 0011 (binary).

2 APQ8064 Overview

The APQ8064 solution's high-level integration significantly reduces the bill-of-material (BOM) to deliver board-area savings. The cost-efficient 28 nm CMOS fabrication technology significantly improves power efficiency for longer wireless connectivity, while enhancing the user's multimedia experience. These factors also reduce product complexity, cost, and time-to-market, despite the added features and functions.

Connectivity/embedded-computing products based upon the APQ8064 chipset may include:

1. Robots
2. Drones
3. Digital Signage Systems
4. Medical Devices
5. Smart Home Hubs
6. Video Conferencing System
7. Security and Surveillance System
8. Gaming Machines and Kiosks
9. Point of Sale Devices
10. Specialized Cameras

The APQ8064 benefits are applied to each of these product types, and include:

- Higher integration to reduce PCB surface area, power consumption, time-to-market, and BOM costs, while adding capabilities and processing power
- Integrated quad applications processor and hardware cores eliminate multimedia coprocessors, providing superior image quality and resolution for mobile devices while extending application times
  - Higher computational power for high-end features
  - DC power savings enable longer run-times
- Position-location and navigation systems are supported via the WGR7640's global navigation satellite system (GNSS) receiver
  - The APQ8064 supports Gen8A (GPS and GLONASS) operation
- A single platform that provides dedicated support for all market-leading codecs and other multimedia formats to support carrier deployments around the world
- DC power reduction using innovative techniques

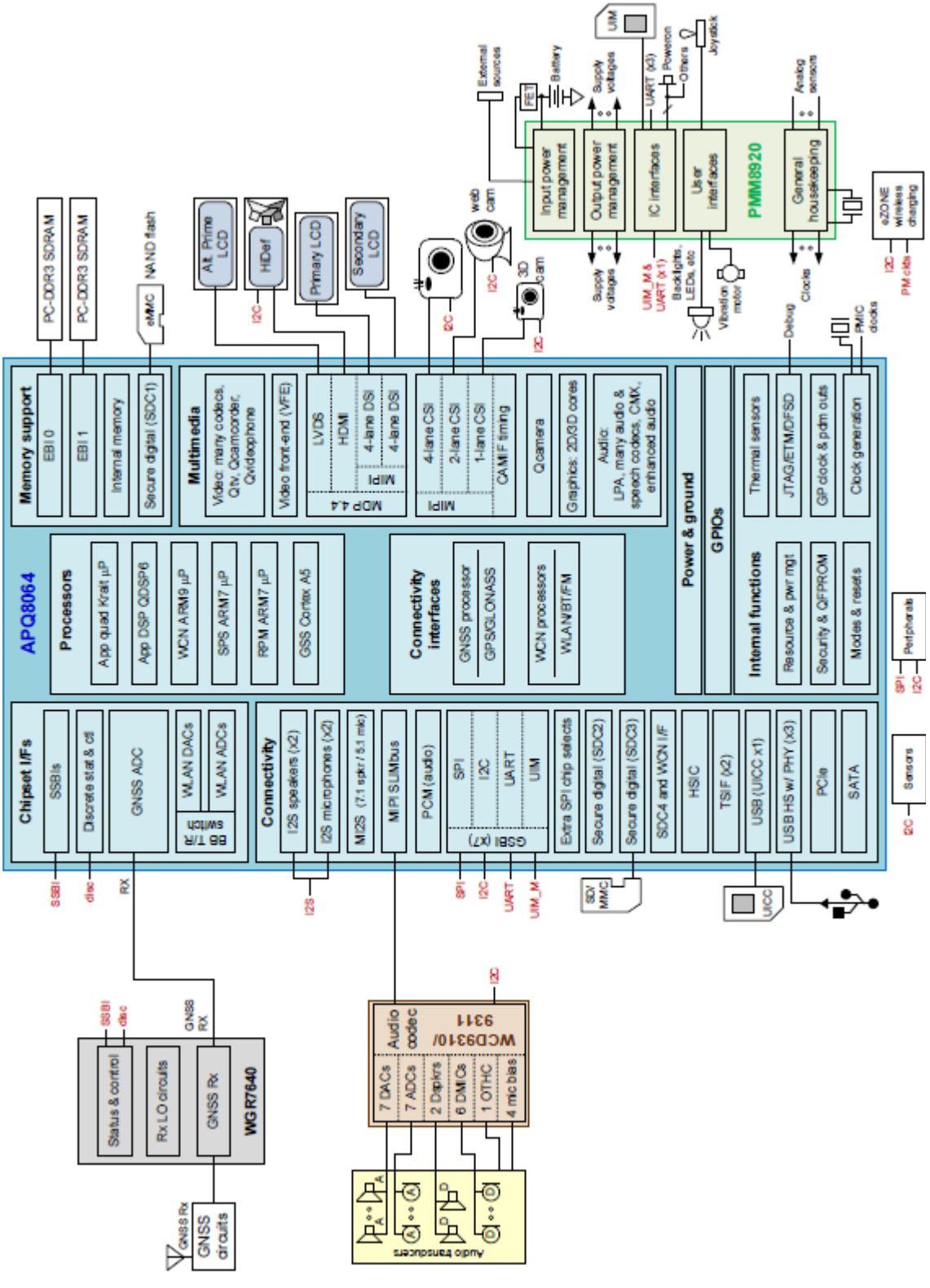

Figure 2-1 APQ8064 functional diagram and example application

Complementary ICs within the APQ8064 chipset include:

- GPS RF receiver: WGR7640
- Power management:
  - PMM8920 IC
- WLAN and FM radio:
  - QCA6234 IC
- Audio codec:
  - WCD9311 IC

The APQ8064 chipset and system-software solution supports the convergence platform for embedded computing applications by leveraging years of expertise. Partners can develop products that meet the exact needs of the growing embedded computing market, providing our customers with complete, verifiable solutions, including fully segmented product families, systems software, testing, and support.

3 Processor Overview

3.1 APQ8064 device features

NOTE Some of the hardware features integrated within the APQ8064 device must be enabled by software. See the latest version of the applicable software release notes to identify the enabled APQ8064 device features.

3.1.1 Architecture and baseband processing features

- Four Krait application processors – advanced CPU architecture for high-end multimedia applications
  - 1.5 to 1.7 GHz (each)
  - 2 MB L2 cache (combined)
  - ARM v7 compliant
  - TrustZone support
  - VeNum 128-bit SIMD multimedia coprocessor
- Powerful QDSP6 core (500 MHz) for application support (within the low-power audio subsystem)
  - 512 kB TCM/L2 memory
- ARM9 for BT/FM processing
- Cortex A5 (256 MHz) for GNSS support (within the global navigation satellite subsystem)
  - ARM v7 compliant
  - 32 kB instruction/data caches
- ARM7 for smart peripheral subsystem processing
- ARM7 for RPM tasks
- ADCs and DACs are integrated into the APQ, plus digital processing for BT, and FM radio
- Smart peripheral subsystem for improved SD and USB transfer rates while offloading the application processor
- Boot flow – RPM/application processor-based
- Primary boot processor is the ARM7 RPM
  - Better suited for code certification and warm boot
  - Brings up the secure root of trust (SROT) Krait processor quickly

3.1.2 Memory support features

3.1.2.1 External PCDDR3 high-speed memory

- Dual-rank, dual-channel PCDDR3 SDRAM, 32-bit wide/channel
- Up to four chip selects (two on EBI0 and two on EBI1)
- Supports up to 4 GB total memory at the 533 MHz clock rate (although a maximum of 3 GB is addressable)
- Other key internal memories
  - 256 kB of local memory (LMEM)
  - 192 kB of multimedia internal memory (MIMEM)
- Secure digital supports eMMC NAND flash
- SPI can be used to support NOR memory devices with appropriate user-modified software

3.1.3 Air interface features

3.1.3.1 Position-location and navigation systems

Table 3-1 Position-location and navigation summary

Standard	Feature descriptions
gpsOne with GNSS support	
Gen8A	■ Global positioning system (GPS) ❒ Next generation gpsOne solution with enhanced GPS engine and low-power tracking ❒ Enhanced navigation 3.0, dynamic power optimization, on-demand positioning, and SBAS (such as WAAS, EGNOS, MSAS) ❒ Support for Wi-Fi positioning ❒ MS/UE-based, MS/UE-assisted, hybrid modes with AFLT (CDMA) and MRL (UMTS), standalone and network-aware modes ❒ gpsOneXTRA Assistance for enhanced standalone GPS performance ❒ Control plane: IS-801, IS-881, and UMTS CP assisted-GPS protocols ❒ User plane: v1/v2 trusted mode and OMA SUPL 1.0 assisted-GPS protocols ❒ Wideband processing of GPS signals helps resolve multipath interference, promoting improved measurement accuracy ■ Support for GLONASS standalone mode ❒ GLONASS capability increases the number of satellites available to the positioning engine, resulting in an expanded area of coverage over traditional GPS receivers

3.1.4 Multimedia features

- Camera interfaces with Qcamera
  - Primary (via 4-lane MIPI_CSI) – supports CMOS and CCD sensors
    - Up to 20 MP in-line JPEG encode at 15 fps
    - 60 fps WXGA viewfinder frame rate

        - A wide variety of pixel manipulation, camera modes, image effects, and post-processing techniques are supported, including *defective pixel correction*.
        - VFE raw dump of CSI data at line rate (4 Gbps) to LPDDR2 or PCDDR3
        - SMIA++ support
        - Plus inter-integrated circuit (I^2C) or SPI control
    - Secondary (via 2-lane MIPI_CSI) – provides webcam functions
        - Up to 8 MP
    - 3D camera (via 1-lane MIPI_CSI)
        - Up to 8 MP
    - In-line JPEG processing
        - No external RAM requirement for image snapshot processing
        - Reduced shot-to-shot latency for multishot photos
- Video applications
    - Qcamcorder – 30 fps at 1080p (H.264/MPEG4); 30 fps at D1 (H.263)
    - Qtv (video decoding)
        - Playback – 30 fps at 1080p (H.264/MPEG2/MPEG4/DivX/VC-1); 30 fps at D1 (H.263)
        - Streaming – 30 fps at 1080p (H.264/MPEG2/MPEG4/DivX/VC-1); 30 fps at D1 (H.263)
    - Qvideophone (VT) – 15 fps at QCIF (MPEG4/H.263)
- Audio codec via the WCD9311
    - I^2S busses or SLIMbus
    - Up to six digital microphones, two speakers, seven ADCs, and seven DACs
- Low-power audio (LPA)
    - Low complexity, low power dissipation
    - 7.1 surround sound
    - Versatile post processing
        - Supports large variety of audio playback and voice modes
        - Encoders for audio recording and FM recording
        - Many concurrency modes are supported
- Audio codecs and audio CMX are supported
    - Audio – MP3, AAC, aacPlus, eAAC, AMR-NB, AMR-WB, G.711, WMA 9/10 Pro
    - CMX – 128 voices, 512 kB wavetable
- Enhanced audio
    - Dolby 5.1 and 7.1 Surround (AC-3)

- Fluence noise cancellation
- QAudioFX/QConcert/QEnsemble

- Audio/visual (A/V) outputs
  - High Definition Multimedia Interface (HDMI Rev. 1.4a)
    - Integrated HDMI Tx core and HDMI PHY
    - 1080p at 60 Hz refresh; 24-bit RGB color
    - Up to 8-channel audio for 7.1 surround sound
    - Dolby Digital Plus, Dolby True-HD, and DTS-HD Master
  - HDMI alternate – Mobile Hi-Definition Link (MHL)
- Mobile display processor (MDP 4.4) with added features and upgraded color correction
- Graphics – optimized specifically for a smaller display screen size and color depth using low-power, high-performance processing
  - Adreno 320 graphics
    - 200 M peak triangles/second
    - 6.4 B vector shader instructions/second
    - 3.2 BP/second; 3.2 B texel/second
  - APIs include OpenGL ES 1.x, 2.0, and 3.0; Direct3D Dx9.x; C2D for 2D composition; OpenCL for Adreno 320
- Display support – up to two concurrent displays
  - Dual display with up to 60 Hz refresh
    - Primary via dual-link MIPI DSI, 1 Gbps per lane, up to QXGA (2048 x 1536)
    - Secondary via 4-lane MIPI DSI, 1 Gbps per lane, up to QHD (960 x 540)
    - Simultaneous dual-display, primary MIPI DSI or LVDS up to QXGA (2048 x 1536), and secondary up to QHD (960 x 540)
    - Alternative primary display via dual LVDS, up to QXGA (2048 x 1536)
  - HDMI (see A/V bullets above)
  - TV output via HDMI
  - Color depth: 24-bit pp
  - Types: TFT, LTPS, CSTN, and OLED
- Web technologies – V8 JavaScript Engine optimizations
  - Webkit browser JPEG hardware decode acceleration
  - Webkit compositing engine 2D/VG GPU acceleration
  - Networking Stack IP and HTTP tuning
  - Flash 10.1 3D/GL-ES GPU acceleration
  - Flash 10.1 and Video Processor/QDSP Video (H.264, VP6, Spark) decode optimization

- Messaging
  - Short messaging services like text messages, text encoding for SMS
  - Multimedia messaging services like combined video (MPEG4), still image (JPEG), voice tag (AMR), and text sent as a message

3.1.5 Connectivity features

- Seven general serial bus interface (GSBI) ports, each up to 4-bits wide; configuration options include:
  - UART
  - UIM
  - I^2C
  - SPI
  - Or GPIO bits
- Universal serial bus (USB)
  - Three USB 2.0 HS ports with built-in PHY (480 Mbps), as a peripheral or embedded host
  - Full-speed USB port for UICC
    - SIM, USIM, and CSIM applications
    - Multimode support for SIM + USIM + CSIM and UMTS support for SIM + USIM
- High-speed inter-chip (HSIC)
  - Easy integration, low power, and low processor loading
- PCI Express (PCIe) interface
  - PCIe 2.0 port, 1x lane
- SATA interface
  - SATA 1.0 port
- Universal asynchronous receiver transmitter (UART) serial ports via GSBI
  - High-speed (UART_DM ports, up to 4 Mbps) and standard UART ports
- User identity module (UIM) ports via GSBI
  - USIM, SIM, and large-capacity (USB-UICC) support (see UICC comments above)
  - Data rates up to 4 MHz
  - 1.8 V support; 3.0 V support with PMIC level translators
- Up to four secure digital controller (SDC) ports
  - Different operating voltages are available, depending on the selected controller
  - 4-bit and 8-bit interfaces are supported
  - MMC and SD cards; eMMC NAND flash memory support; eSD/eMMC boot
  - SDC3 support dual-voltage (1.8 V and 2.9 V) SD card interface

  - Supports both SD version 3.0 and MMC version 4.4.1/4.5
- I^2C ports for peripheral devices via GSBI
  - 1.8 V interfaces
  - Controls for some of the chipset ICs
  - Camera sensor/module controls and other sensors
  - NFC
- Up to eight multiple inter-IC sound (MI^2S) interfaces
  - Supports microphone and speaker functions, including 7.1 audio for HDMI
- Serial peripheral interface (SPI) ports via GSBI
  - SPI master supports up to a 52 MHz output clock
  - Camera sensor/module controls
  - External sensors and audio
  - NOR memory support (with user-modified software)
- Pulse coded modulation (PCM) interface
- Touch screen
  - Supports an external touch screen controller IC, via the I^2C or SPI interface, and interrupts

3.1.6 Configurable GPIO features

- 90 GPIO pins (GPIO_0 to GPIO_89)
- Input configurations: pull-up, pull-down, keeper, or no-pull
- Output configurations: programmable drive current
- Top-level mode multiplexer (TLMM) provides a convenient way to program groups of GPIOs

3.1.7 Features of internal functions

- Key security features include secure boot, secure file system (SFS), OMA DRM 1.0/2.1, ARM TrustZone, SecureAPQ v3, Microsoft Windows Mobile DRM10 and HDCP for HDMI
- Crypto Engine V4 with algorithms that accelerate file system encryption (AES-XTS) and IPSec and SSL (HMAC-SHA, CCM, CBCMAC)
- New security controller and enhanced QUALCOMM Fuse Programmable Read Only Memory (QFPROM)
  - Handles chip-wide configuration for security, feature enabling, and debugging; provides persistent storage of ID numbers and sensitive key data
  - The enhanced Qfuse cells are a large fuse array that replaces previous-generation fuse chains as the IC's nonvolatile memory elements; much faster and simpler programming

- Secure HDCP key provisioning and secure debug facility that creates a secure tester channel for provisioning key information or enabling features and debug capabilities; also provides a gateway for all software and JTAG accesses to the Qfuse
- Support for the HDCP standard needed for HDMI
  - HDCP key interface between the HDCP encoder and the Qfuse (HDCP key is only readable through this interface)
- Primary and secondary hardware key blocking for the secure file system

- Boot sequence: 1) RPM system, 2) applications system, and then 3) other processor subsystem
  - Emergency boot over HS-USB is supported
  - Boot time from poweron to carrier splash screen is less than 0.4 seconds (target)
  - Boot time from poweron to network access is less than 20 seconds (target)
- PLLs and clock generation/distribution
  - 19.2 MHz CXO, 27 MHz PXO, 48 MHz WCN_XO, and 32.768 kHz sleep clock inputs
  - Multiple internal clock regimes
  - General-purpose clock, M/N counter, and PDM outputs
  - Internal watchdog and sleep timers
- RPM functions for improved efficiency
  - Fundamental to boot-up and power management
  - Key functional blocks include the RPM core and its ARM7 processor, the security control core
  - Shuts down clock sources or reduces clock rates; performs power collapse or voltage scaling, including split-rail core and memory supply voltages; supports several low-power sleep modes
  - Enables new boot sequences compared to previous-generation APQs
- Smart peripheral subsystem – ARM7-based core that enables the *sensor always-on* capability without requiring the application subsystem to be on (reduces DC power)
- Thermal sensors
- Modes and resets
- Debug – JTAG/ETM/design for software debug (DFSD)
  - ETM from all cores

3.1.8 Chipset interface features

- Wireless GPS receiver (WGR) interfaces
  - Rx analog baseband from WGR to APQ ADC
  - Clock from PMM8920
  - SSBI

- Dedicated status and control lines as needed
- Audio codec to/from the WCD
  - SLIMbus for highly multiplexed, high-speed audio data
  - I^2C for primary status and control
  - Plus dedicated status and control lines as needed
- Wireless connectivity network (WCN) interfaces
  - BT – data, clock, and SSBI
  - FM radio – data and SSBI
  - Plus dedicated status and control lines as needed
- PMIC status and control (PMM8920)
  - SSBI
  - Interrupt ports and other dedicated clock and control signals
- Housekeeping ADC and analog multiplexer
  - Integrated into the PMM8920

3.1.9 Summary of key APQ8064 features

Table 3-2 Key APQ8064 features

Feature	APQ8064 capability
Processors	
Processors Applications subsystem RPM system Smart peripheral subsystem BT/FM GPS subsystem	 Four Krait mP cores (to 1.7 GHz) plus one QDSP6 core (to 500 MHz) ARM7 ARM7 ARM9 Cortex A5
Memory support	
External memory Via EBI Via SDC interface Via SPI	 533 MHz; 32-bit; up to 4 Gbit density PCDDR3 eMMC/SD devices NOR memory devices (requires user-modified software) 384 kB of LMEM
Other internal memory	384 kB of LMEM 192 kB of MIMEM
RF support	
GNSS – supported features	gpsOne; standalone, MS-A, MS-B, and GLONASS

Table 3-2 Key APQ8064 features (Continued)

Feature	APQ8064 capability
Multimedia	
Camera interfaces	Qcamera; 20 MP
Primary	4-lane MIPI_CSI – 20 MP; 60 fps WXGA viewfinder frame rate
Secondary	2-lane MIPI_CSI – 8 MP; webcam support
Tertiary	1-lane MIPI_CSI - 8 MP; 3D support
In-line JPEG	Reduced shot-to-shot latency for multi-shot photos
Video applications performance	
Qcamcorder	30 fps at 1080p (H.264/MPEG4); 30 fps at D1 (H.263)
Qtv	
Playback	30 fps 1080p (H.264/MPEG2/4/DivX/VC-1); 30 fps D1 (H.263)
Streaming	30 fps 1080p (H.264/MPEG2/4/DivX/VC-1); 30 fps at D1 (H.263)
Qvideophone	15 fps at QCIF (MPEG4/H.263)
Audio	
Codec	Integrated within the WCD Up to 6 digital microphones, 2 speakers, 7 ADCs, and 7 DACs
Low-power audio	Low-power, low-complexity; versatile post-processing; 7.1 surround
Synthesizer	128-voice polyphony wavetable
A/V outputs	
HDMI Rev 1.4a (or MHL)	Integrated HDMI Tx core and HDMI PHY 1080 p at 60 Hz refresh; 24-bit RGB color Up to 8-channel audio for 7.1 surround sound Dolby Digital Plus, Dolby True-HD, and DTS-HD Master
2D/3D graphics acceleration	Adreno 320 graphics: 200 M peak triangles/sec; 6.4 B vector shader instructions/sec; 3.2 BP/sec; 3.2 B texel/sec APIs include OpenGL ES 1.x, 2.0, and 3.0; Direct3D Dx9.x; C2D for 2D composition; OpenCL for Adreno 320
Display support	Up to three concurrent displays
Primary	Dual-link MIPI DSI – up to WQXGA (2560 x 1600), up to 60 Hz refresh
Alternate primary	LVDS – up to WQXGA (2560 x 1600); dual channel
Secondary	4-lane MIPI DSI – up to QHD (960 × 540), up to 60 Hz refresh
Simultaneous display	Primary via 4-lane MIPI DSI or LVDS, up to QXGA (2048 x 1536); secondary via 3-lane MIPI DSI, up to QHD (960 × 540); plus external display
Tertiary	HDMI/MHL
Mobile display processor (MDP)	MDP 4.4
Connectivity	
GSBI ports	Seven, 4 bits each; multiplexed serial interface functions
USB interfaces	Thee USB 2.0 HS with built-in PHY One USB 2.0 HSIC One USB 2.0 FS for UICC only
PCIe interface	PCIe 2.0, 1-lane
SATA interface	SATA 1.0

Table 3-2 Key APQ8064 features (Continued)

Feature	APQ8064 capability
UART interfaces	Via GSBI
UIM support	Via GSBI; SIM+USIM+CSIM and SIM+USIM
Secure digital interfaces	Up to four ports; MMC and SD cards; eMMC NAND flash; SD/eMMC boot
I^2C interfaces	Via GSBI; some chipset IC controls; camera controls; NFC; etc.
I^2S interfaces	Supports external audio devices
SLIMbus	Audio interfaces with the WCD9311
SPI (master only)	Via GSBI; up to 52 MHz; sensor/module controls; other applications
PCM	Available
TSIF	Up to two ports
Touch screen support Capacitive panels	 Via external IC (I2C, SPI, and interrupts)
NFC	With external NFC device via I2C
Internal functions	
Security	Secure boot, SFS, OMA DRM 1.0/2.1, ARM TrustZone, SecureAPQ v3, Microsoft Windows Mobile DRM10 and HDCP for HDMI, new security controller and enhanced Qfuse
Resource and power manager	Improved efficiency via clock control, split-rail power collapse and voltage scaling, supports several low-power sleep modes New boot sequences compared to previous-generation APQs: 1) RPM system, 2) applications system, and then 3) other processor subsystem

3.2 Krait microprocessor subsystem

- Newer, faster, and more power efficient Krait cores
- Latest ARMv7 architecture extensions
  - Virtualization
  - 36-bit physical addressing
- QGIC2 interrupt controller includes virtualization extension
- ARM generic timer (QTIMER)
- 2nd-generation SAW (SAW2)
- Dynamic power management using SAW2
- New address map to support security requirements
- Quad Krait mP CPUs, each with:
  - Up to 1.7 GHz

- 2 MB L2 cache
- 32 kB L1 instruction and data caches
- ARM v7 compliant
- TrustZone support
- VeNum 128-bit SIMD MM coprocessor

- Shared L2 Cache
  - 2 MB, 8-way set associative with ECC
  - HW-enforced coherency, including slave port
  - Dual interleaved AXI master ports increase memory BW
  - L2 lines individually lockable to create virtual TCM
- KMSS AHB
  - 32-bit at 66 MHz
  - Local connection from CPUs to memory
  - High-BW multimedia traffic mostly localized to separate multimedia fabric
  - Tiered arbitration to enable efficient bus/memory sharing with priority for CPUs
- SDRAM memory
  - See Chapter 4 – Memory Map
- Multiple power and clock domains
  - Independent domains for µP1, µP2, µP3, µP4, and memories
  - L2 data retention enables CPU power-collapse
  - Independently scalable clocks for each core and L2

3.3 Multimedia subsystem

- Major blocks:
  - Display support (red)
  - Image processing (green)
  - Graphics (orange)
  - Audio
- Graphics acceleration HW
  - Adreno 320 3D graphics engine improves user interface, browsing, and gaming performance
  - API support including Open VG, Open GL ES 2.0, etc.
  - Tiled 3D GPU architecture with 512 kB memory reduces DDR bandwidth requirements
- Other multimedia acceleration HW

- JPEG encode & JPEG decode
- Video pre-processing (VPE)
- Display pre-processing
- Display engine with in-line processing for HDMI support

- Advanced bus fabric
  - 128-bit wide fabric at 166 MHz for high-BW access to local multimedia memories
  - Tiered arbitration enables efficient sharing of bus and memories
- Encoder/decoder acceleration HW
  - Multi-format decoder and encoder support up to 1080p at 30 fps
  - Encode/decode function fully offloaded from applications CPUs
  - Improves video performance for applications like broadcast TV, movie playback, web browsing, camcorder, etc.
- Multimedia DDR memory
  - See Chapter 4 – Memory Map

3.4 Low-power audio subsystem

- Power efficient audio processing
  - New QDSP6v4 core
  - New SLIMbus interfaces
    - Approximately 24 Mbps of uncompressed audio data bandwidth
    - SLIMbus includes customized slew-rate limited IOs
  - Support for up to 6 digital microphones
- Low power features:
  - Power gating within LPASS core
  - QDSP6 supports L2 cache data retention during power collapse
  - Supported modes: ACTIVE / IDLE / DORMANT / OFF
- Local clock control with dedicated PLL
- Low-power memory
  - Dedicated SRAM
  - Bitstream buffer, PCM buffers, DSP OS
- Musical Instrument Digital Interface (MIDI)
  - Acceleration HW
  - 128-poly MIDI processing

- Audio DSP
  - Near-zero cache miss-rates during steady-state low-power audio playback
  - Separate voltage domain is scaled with performance requirements
- PCM, DMIC, MI^{2}S/I^{2}S legacy low-power audio interfaces

3.5 Smart peripheral subsystem

Improves peripheral operations requiring significant main CPU and system DRAM involvement (high loading) - power optimized architecture for higher throughput at lower power dissipation.

- Decentralized, very scalable architecture
- High throughput peripheral devices are concentrated in a semi-autonomous subsystem

- General SPSS Features
  - HW clock gating
  - Dedicated busses with performance monitoring
  - Security features based on Virtual Master ID implementation
  - Dynamic bus scaling (HS-USB requires 60 MHz+)
- DMA Accelerator interface
- Pipe memory
  - Producers and consumers communicate via unidirectional pipes
  - Memory and configuration parameters
- Sensor processor
  - ARM7 up to 64 MHz with 176 kB TCM
- Bus access manager (BAM)
  - Manages data transfers between the peripheral and the pipe memory
- Crypto4
  - Used to encrypt/decrypt content to/from SD and USB devices
- Sensor-specific Features
  - Centralized hub with dedicated memory
  - Interfaces for several sensors, different types
  - BOM reduction, low cost sensors
  - Low latency response
  - Reduced software complexity
  - 24 x 7 Applications such as pedometer

3.6 Chip peripheral subsystem

3.6.1 USB features

USB interfaces are supported by two controller types.

- The primary controller is the HS-USB port with an integrated physical layer (PHY). This port is also capable of supporting USB operations at low-speed and full-speed.

Additional USB information is available at www.usb.org/developers/

3.6.2 TSIF features

- APQ8064 has two Transport Stream Interfaces for communication with broadcast or similar ICs
  - Each TSIF bus consists of:
    - CLK, Data, En and Sync lines
- TSI format is specified by IEC 13818-1 and is the MPEG 2 TS format
- Frequency is 27MHz

4 Memory Map

The system memory map is shown in the next figure.

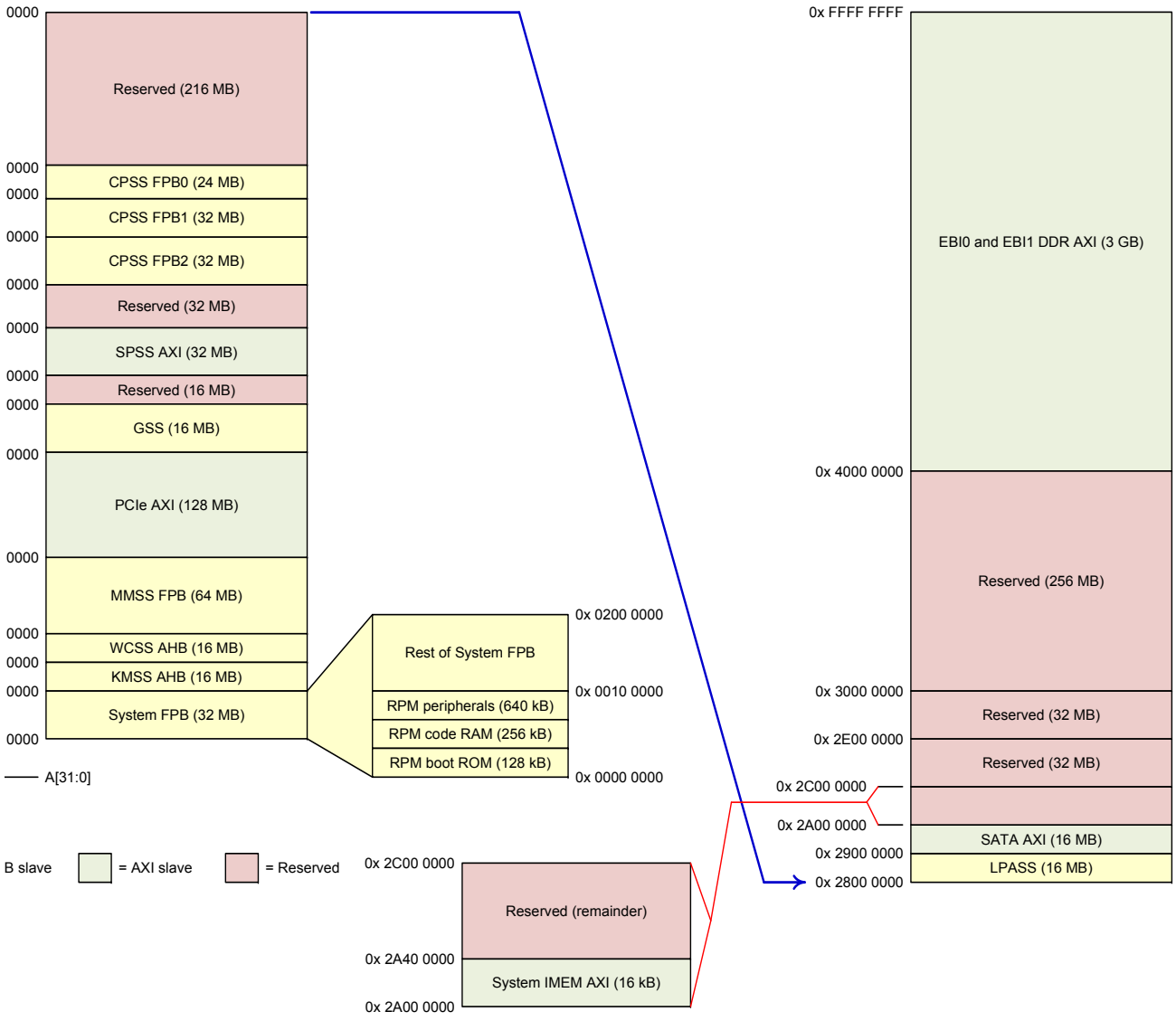

Figure 4-1 Memory map

4.1 Memory controller

See Chapter 12 – Memory controller

4.2 eMMC NAND flash on SDC

eMMC is used to boot the device.

See Chapter 12 – eMMC NAND flash on SDIO

5 Device Support

See the Introduction (Chapter 1 – Introduction) for information on development support tools for the APQ8064 chipset.

6 Device Configurations

6.1 System module registers

6.2 Boot modes

Table 6-1 BOOT_CONFIG pin options 1 through 5

Option	FAST_ BOOT_ SELECT fuse	OEM_ SECURE_ BOOTn fuse	BOOT_ CONFIG [6] GPIO status	BOOT_CONFIG[5:0] GPIO status	Secure boot enabled	Advantages and use-case
1	Blown	Blown	Don't care	1. BOOT_CONFIG[5:0] pin state is ignored. 2. BOOT_CONFIG pins can be re-purposed as GPIOs. 3. Fast boot device is selected by the FAST_BOOT_SELECT fuse blown values set by software. 4. SECURE_BOOT configuration is controlled by the OEM_SECURE_BOOTn (n = 1...28) fuse settings. 5. AUTH_EN, TABLE_SEL, and KEY_SEL bits of the enabled configuration are selected by blowing these bits of the selected OEM_SECURE_BOOTn fuse settings. 6. OEM_SECURE_BOOT1 is supported.	Yes **Recommended solution for production environment**	Fixed, most secure and recommended solution for production environment. Less components are required (removal of pull-ups on BOOT_CONFIG pins), reduces BOM cost and PCB area.
2	Not blown	Not blown	1	1. Fast boot device is selected by BOOT_CONFIG[4:0] combinations as shown in Table 6-2. 2. BOOT_CONFIG[5] is not used.	No	Allows boot device flexibility (for example, USB vs. eMMC) and is intended for use in R&D stage. Device boots up in non-secure mode.
3	Not blown	Blown	1	1. Fast boot device is selected by BOOT_CONFIG[4:0] combinations as shown in the Table 6-2. 2. BOOT_CONFIG[5] is not used. 3. Secure Boot Authentication is controlled by OEM_SECURE_BOOTn fuses.	Yes	Allows boot device flexibility (for example, USB vs. eMMC) and is intended for use in R&D stage. Device boots up in secure mode.

Table 6-1 BOOT_CONFIG pin options 1 through 5 (Continued)

Option	FAST_ BOOT_ SELECT fuse	OEM_ SECURE_ BOOTn fuse	BOOT_ CONFIG [6] GPIO status	BOOT_CONFIG[5:0] GPIO status	Secure boot enabled	Advantages and use-case
4	Blown	Not blown	0	1. Status of BOOT_CONFIG[4:0] pins as shown in the Table 6-3 determines which OEM_SECURE_BOOTn region is turned on by selecting the specific AUTH_EN bit of that region. **Note:** In option 1 – AUTH_EN bit is blown in the fuse settings. 2. OEM_SECURE_BOOT1 is supported. 3. TABLE_SEL and KEY_SEL bits of the enabled configuration are selected by blowing these bits in the OEM_SECURE_BOOTn fuse settings. 4. Fast boot device is selected by the FAST_BOOT_SELECT fuse blown values set by software.	Yes	Recommended to be used for a fixed boot device (example – eMMC only) and for authentication testing in R&D stage. Device boots up in secure mode if the OEM_SECURE_BOOT1 region is turned on.
5	Not blown	Blown	0	1. Status of BOOT_CONFIG[4:0] pins as shown on the Table 6-2 determines which OEM_SECURE_BOOTn region is turned on by selecting the specific AUTH_EN bit of that region. **Note:** In option 1 – AUTH_EN bit is blown in the fuse settings. 2. OEM_SECURE_BOOT1 is supported. Refer to Note 1 on the Table 6-2. 3. TABLE_SEL and KEY_SEL bits of the enabled configuration are selected by blowing these bits in the OEM_SECURE_BOOTn fuse settings. 4. Fast boot device is the default boot device (SDC3).	Yes	Device boots up with the default boot device (SDC3). Boot device cannot be changed. Device boots up in secure mode if the OEM_SECURE_BOOT1 region is turned on.

Table 6-2 Fast boot device selection by BOOT_CONFIG GPIOs

BOOT_CONFIG[5:0]	BOOT_CONFIG[6] = 1 = fast boot
0b000000	SDC3 followed by HS-USB
0b000001	SDC3 followed by SDC1
0b000010	SDC3 followed by SDC2
0b000011	SDC1(eMMC)
0b000100	SDC2

Table 6-3 Secure boot device selection by BOOT_CONFIG GPIOs

BOOT_CONFIG[5:0]	BOOT_CONFIG[6] = 0 = secure boot
0b000000	No secure boot, as BOOT_CONFIG[4:0] = 0
0b000001	Secure boot1 from OEM_SECURE_BOOT1 configuration
0b000010	Secure boot2 from OEM_SECURE_BOOT2 configuration
0b000011	Secure boot3 from OEM_SECURE_BOOT3 configuration
0b000100	Secure boot4 from OEM_SECURE_BOOT4 configuration

6.3 Device clocking

6.3.1 Clock architecture

Figure 6-1shows the APQ8064 clock architecture.

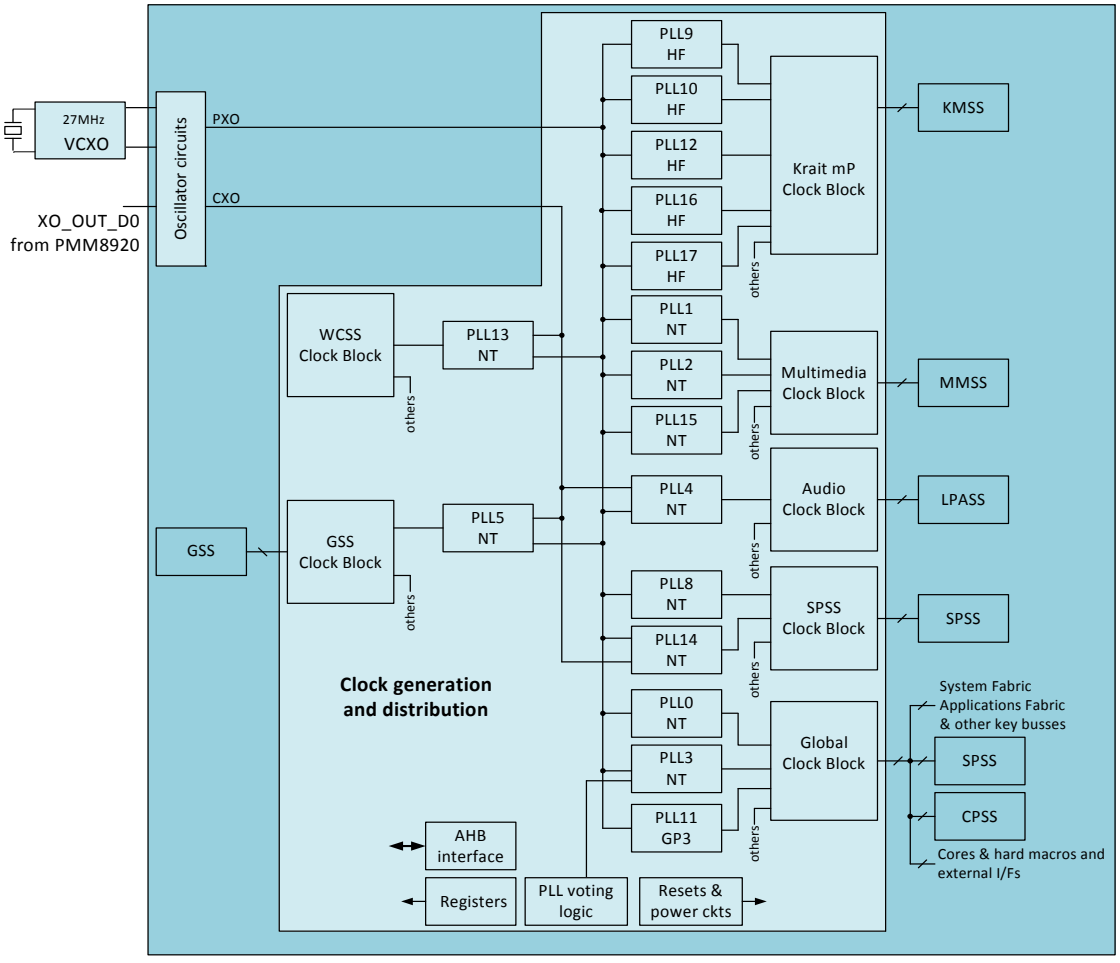

Figure 6-1 Clock architecture

NOTE PLL13 is only used if the WCN3660 XO is not used.

6.3.2 Phase-locked loops

- Types
  - General purpose (GP3)
  - Low power (NT)
  - High frequency (HF)
- Four PLLs have an option to use CXO, all others use PXO
- 16 PLLs total

6.3.3 Clock blocks

- Inputs – oscillator signals, PLL signals, and test sources.
- Various clock-circuit types generate all clocks needed by the system.
- Clock outputs are organized into clock regimes.
- Three clock blocks are dedicated to specific systems or subsystems.
- One clock block serves multiple systems and subsystems, in addition to buses, hardware cores, hard macros, and external interfaces.

6.3.4 Clock regimes

- Collections of clock signals that drive sets of circuit cores or blocks having similar clock requirements

Table 6-4 Clock regimes

Clock regime	Highest frequency	Frequency range
Apps fabric	533 MHz turbo mode 400 MHz normal	27 to 533 MHz; other selections available within this range
System fabric	160 MHz normal mode	Integer divide of different PLLs
SPSS fabric	64 MHz	64 MHz and integer divide of PLL8
RPM system FPB	64 MHz	64 MHz and integer divide of PLL8
CPSS FPBs	64 MHz	64 MHz and integer divide of PLL8
Multimedia fabric	220 MHz	200 MHz and integer divide of PLL8
MMSS FPB	83 MHz	83 MHz and integer divide of PLL8
EBI	533 MHz	27 to 533 MHz; other selections available within this range

6.3.5 Supported by digital control functions

- AHB interface, registers, reset circuits, and power control circuits – enables subsystem configuration, control, and status
- PLL voting logic – processors cast votes to enable their PLL(s); vote-to-enable scheme prevents one processor from denying another processor's PLL; state machine implements control without software intervention

6.4 Power and sleep control

For information on power control, see Chapter 10 – Power management.

Four types of sleep modes reduce APQ leakage current:

1. Clock off
   - Clock sources (CXO and PXO) are turned off, but the core and memory power-supply voltages operate normally.
   - Upon wakeup, one of the interrupt sources is triggered, and then forwards the interrupt to other parts of the RPM system.
2. Core and memory supply voltages minimized
   - Up to four preprogrammed SSBI commands are sent to the PMIC to initiate the shutdown or wakeup process.
   - Core supply voltage is reduced first, and then the memory supply voltage.
   - Memory states and logic states are preserved.
   - Clocks are also turned off.
3. Core power-supply voltage collapsed and memory supply voltage minimized (but still on)
   - Pertinent comments from #2 above apply, except the following:
     - Core voltage is collapsed, not just minimized.
     - Memory contents are retained, but logic states are lost.
4. Full IC power collapse (core and memory supply voltages collapsed)
   - Pertinent comments from #2 above apply, except the following:
     - Both voltages are collapsed, not just minimized.
   - Lowest leakage current, but requires saving and restoring necessary states.
   - Software overhead and complexity are significant.LM80-P0598-1 Rev. B

6.5 Pin multiplexing

6.5.1 I/O parameter definitions

Table 6-5 I/O description (pad type) parameters

Symbol	Description
Pad attribute	
AI	Analog input (does not include pad circuitry)
AO	Analog output (does not include pad circuitry)
B	Bidirectional digital with CMOS input
DI	Digital input (CMOS)
DO	Digital output (CMOS)
H	High-voltage tolerant
S	Schmitt trigger input
Z	High-impedance (high-Z) output
Pad-pull details for digital I/Os	
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters and is a prefix to other programmable options: NP: pdpukp = default no-pull with programmable options following the colon (:) PD: nppukp = default pull-down with programmable options following the colon (:) PU: nppdkp = default pull-up with programmable options following the colon (:) KP: nppdpu = default keeper with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
NP	Contains no internal pull
PU	Contains an internal pull-up device
PD	Contains an internal pull-down device
Pad voltage groupings for baseband circuits	
P1	Pad group 1 (EBI0 and EBI1); tied to VDD_P1 pins (1.2 V only)
P2	Pad group 2 (SDC3); tied to VDD_P2 pins (1.8 V or 2.85 V)
P3	Pad group 3 (most peripherals); tied to VDD_P3 pins (1.8 V only)
P4	Pad group 4 (HSIC); tied to VDD_P4 pins (1.8 V only)
Output current drive strength	
EBI0 and EBI1 pads	Pads for EBI0 and EBI1 are tailored for 1.2 V interfaces and are source terminated. At the pads, after the source termination, the drive strength at I_{OL}, I_{OH} is equivalent to a range of 0.8 to 2.5 mA in nonlinear steps when the JEDEC standard range (90%/10%) is followed.
3.0 V (H) pads	Programmable drive strength, 2 to 8 mA in 2 mA steps
Others [a]	Programmable drive strength, 2 to 16 mA in 2 mA steps

a. Digital pads other than EBI0 and EBI1 pads, or high-voltage tolerant pads.

6.5.2 Pin assignments – APQ bottom

The APQ8064 device is available in the 784-pin flip-chip BGA package (784 FCBGA) that includes several ground pins for electrical grounding, mechanical strength, and thermal continuity. A high-level view of the pin assignments is shown in the figure below.

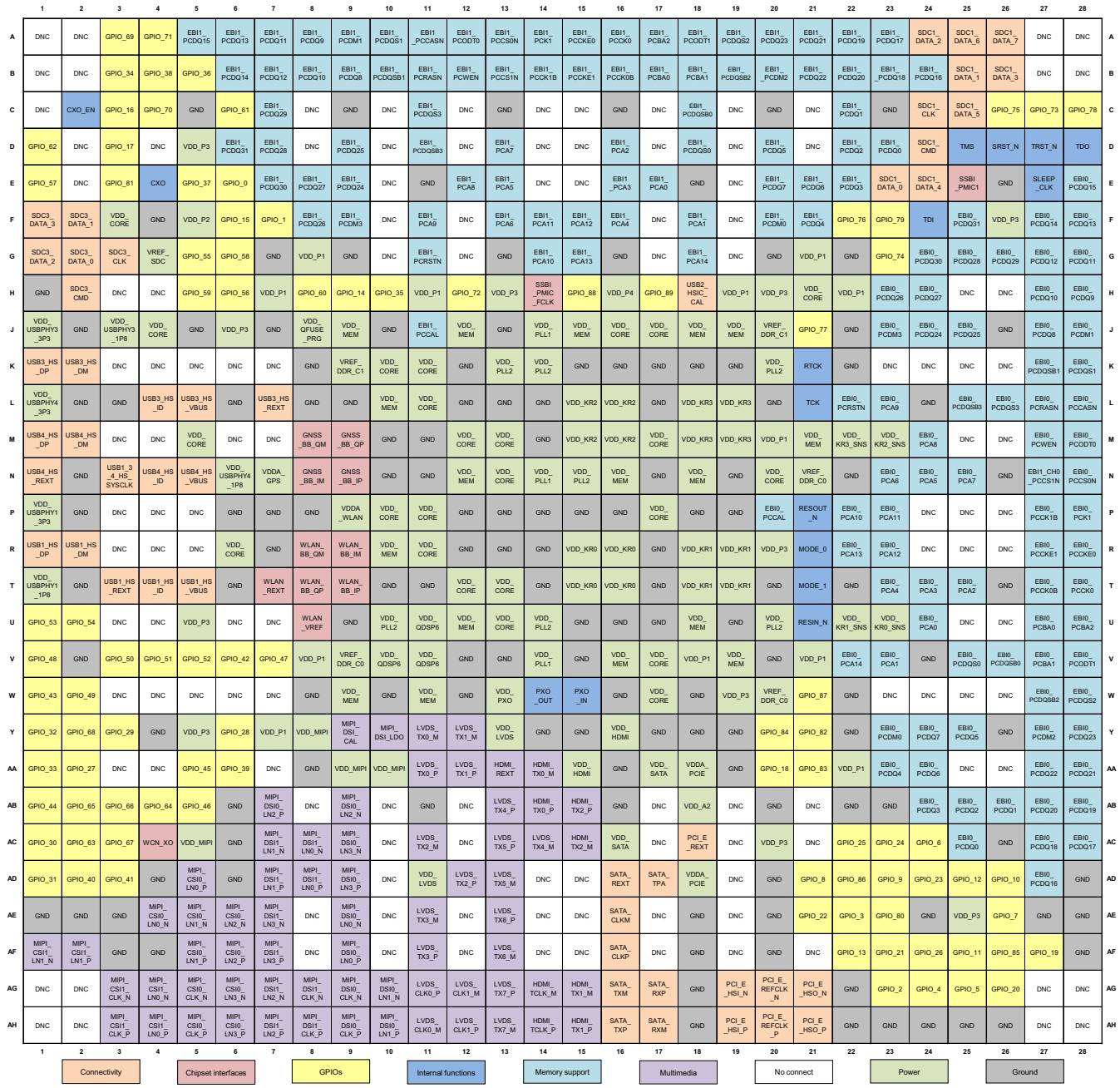

Figure 6-2 APQ8064 pin assignments (top view)

Since the text within Figure 6-2 above is very difficult to read, six close-up views are shown in the following figures.

Figure 6-3 APQ8064 pin assignments – upper left quadrant

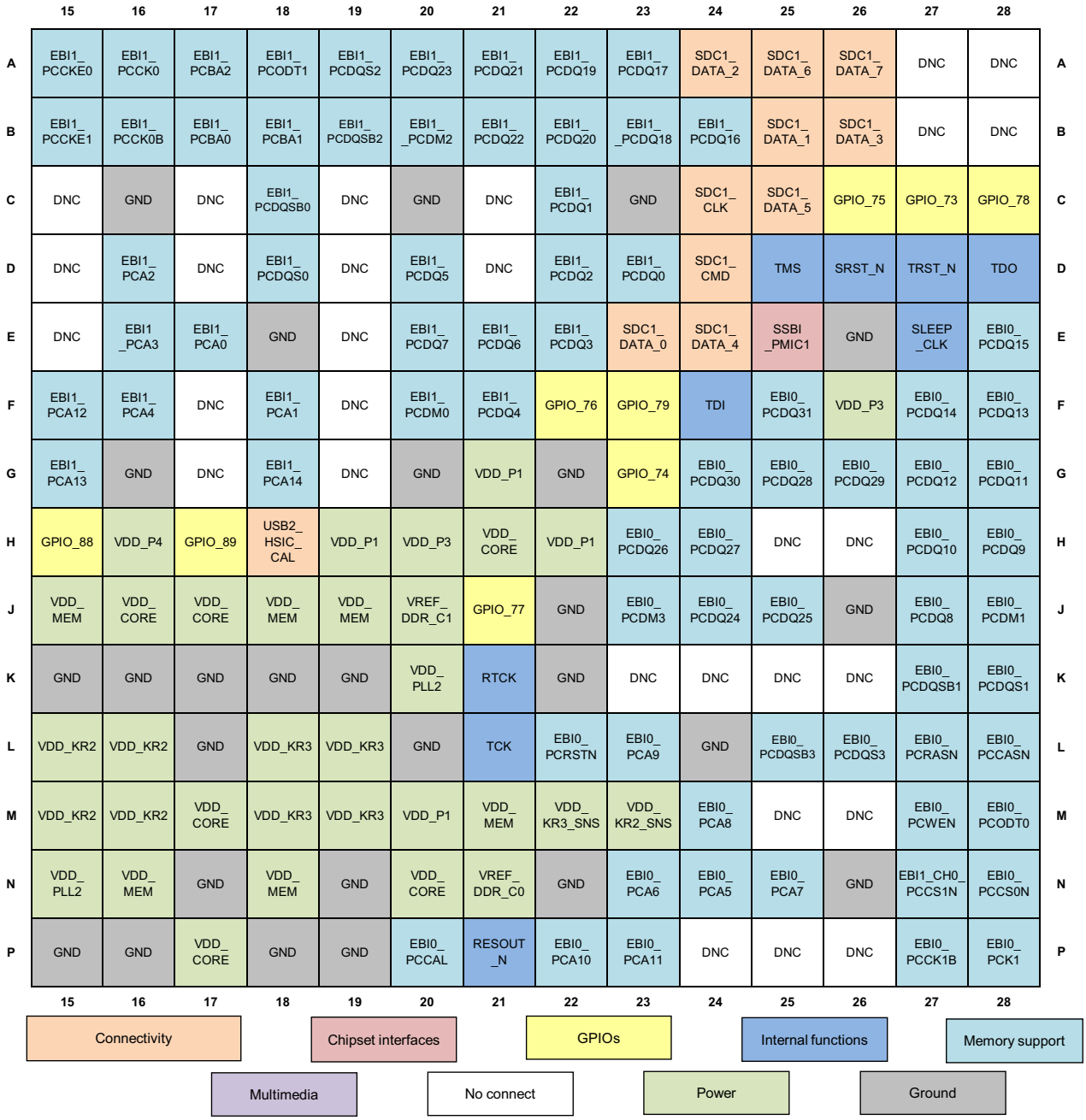

Figure 6-4 APQ8064 pin assignments – upper right quadrant

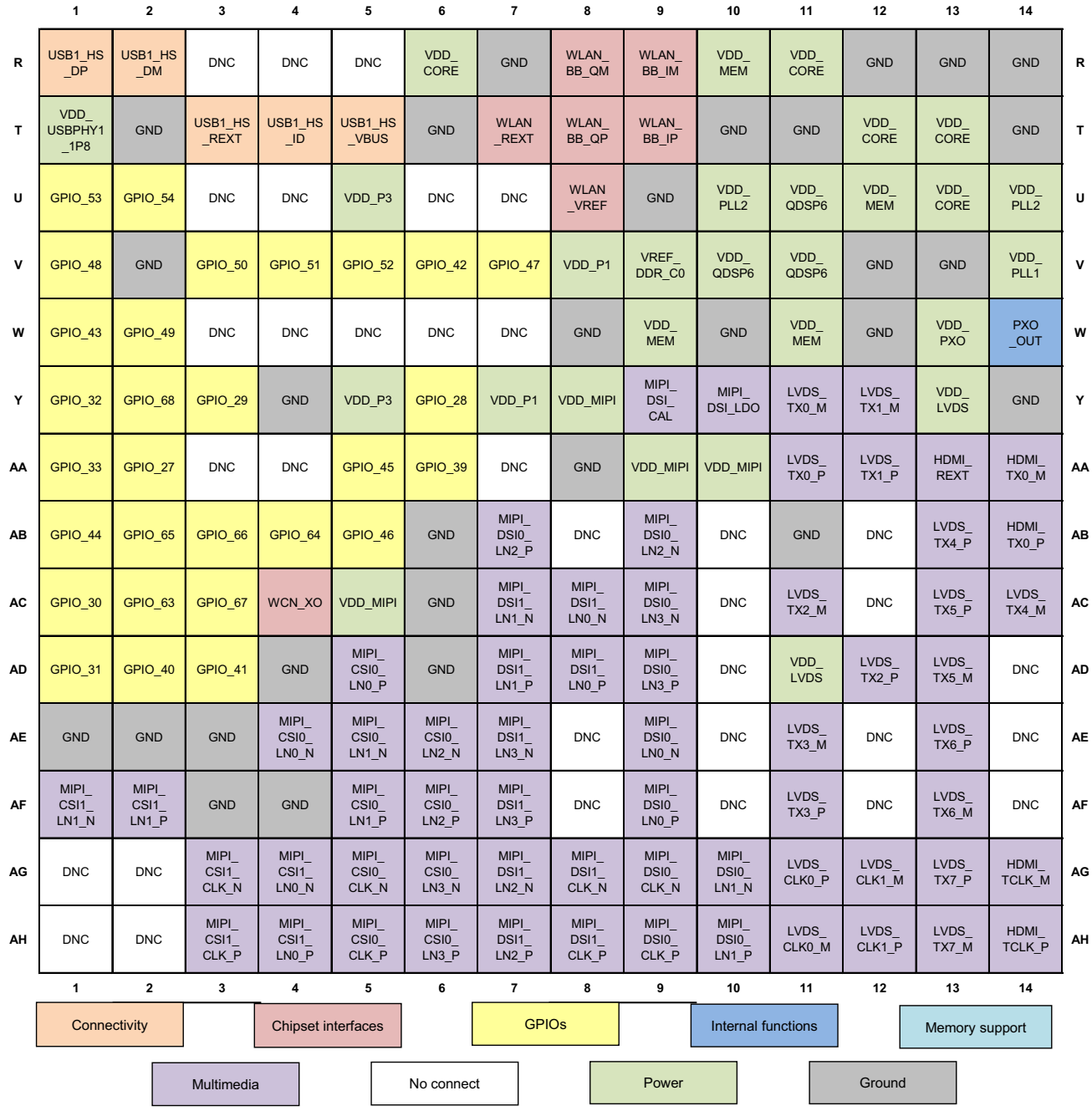

Figure 6-5 APQ8064 pin assignments – lower left quadrant

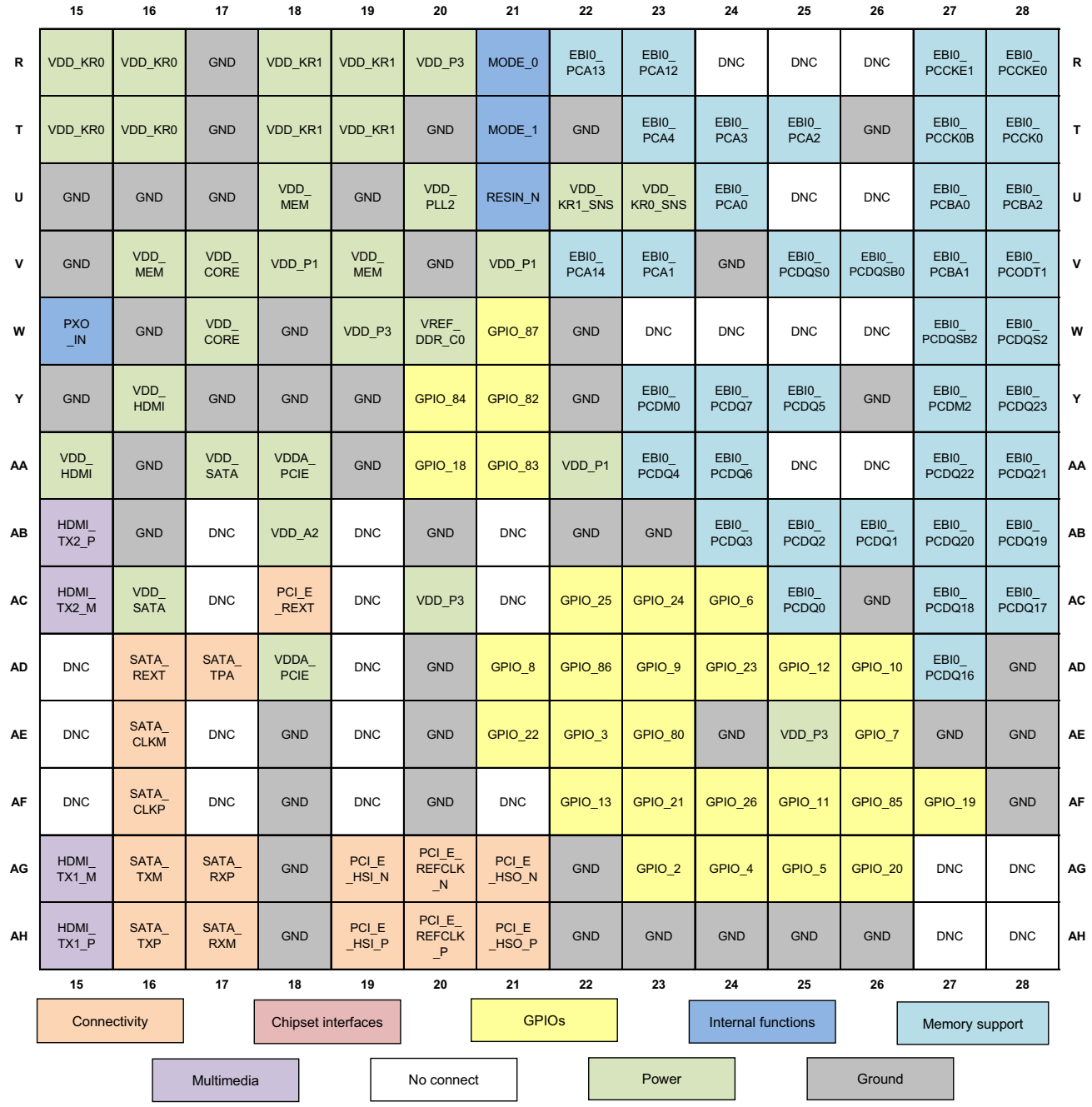

Figure 6-6 APQ8064 pin assignments – lower right quadrant

6.5.3 Pin descriptions

Descriptions of bottom pins are presented in the following tables, organized by functional group:

Table 6-6 Memory support functions

Table 6-7 Multimedia functions

Table 6-8 Connectivity functions

Table 6-9 Internal functions

Table 6-10 Wakeup pins

Table 6-11 Chipset interface functions

General-purpose input/output ports - see Chapter 11 – GPIO.

GSBI configurations – twelve 4-pin sets of GPIOs are available as general serial bus interface ports that can be configured for UART, UIM, SPI, or I2C operation- see Chapter 11 – GPIO.

Table 6-12 No connection, do not connect, and reserved pins

Table 6-13 Power supply pins

Table 6-14 Ground pins

Table 6-6 APQ8064 pin descriptions – memory support functions

Pad #	Pad name and/or function	Pad name or alt function	Pad voltage	Pad type	Functional description
EBI1 for PCDDR3 SDRAM block 1, channel 0					
U24	EBI0_PCA0		P1	DO	PCDDR3 block 1, channel 0 command/address bit 0
V23	EBI0_PCA1		P1	DO	PCDDR3 block 1, channel 0 command/address bit 1
T25	EBI0_PCA2		P1	DO	PCDDR3 block 1, channel 0 command/address bit 2
T24	EBI0_PCA3		P1	DO	PCDDR3 block 1, channel 0 command/address bit 3
T23	EBI0_PCA4		P1	DO	PCDDR3 block 1, channel 0 command/address bit 4
N24	EBI0_PCA5		P1	DO	PCDDR3 block 1, channel 0 command/address bit 5
N23	EBI0_PCA6		P1	DO	PCDDR3 block 1, channel 0 command/address bit 6
N25	EBI0_PCA7		P1	DO	PCDDR3 block 1, channel 0 command/address bit 7
M24	EBI0_PCA8		P1	DO	PCDDR3 block 1, channel 0 command/address bit 8
L23	EBI0_PCA9		P1	DO	PCDDR3 block 1, channel 0 command/address bit 9
P22	EBI0_PCA10		P1	B	PCDDR3 block 1, channel 0 command/address bit 10
P23	EBI0_PCA11		P1	B	PCDDR3 block 1, channel 0 command/address bit 11
R23	EBI0_PCA12		P1	B	PCDDR3 block 1, channel 0 command/address bit 12
R22	EBI0_PCA13		P1	B	PCDDR3 block 1, channel 0 command/address bit 13
V22	EBI0_PCA14		P1	B	PCDDR3 block 1, channel 0 command/address bit 14
U27	EBI0_PCBA0		P1	B	PCDDR3 block 1, channel 0 byte access bit 0
V27	EBI0_PCBA1		P1	B	PCDDR3 block 1, channel 0 byte access bit 1
U28	EBI0_PCBA2		P1	B	PCDDR3 block 1, channel 0 byte access bit 2
P20	EBI0_PCCAL		P1	B	PCDDR3 block 1, channel 0 I/O calibration pad
L28	EBI0_PCCASN		P1	B	PCDDR3 block 1, channel 0 CAS

Table 6-6 APQ8064 pin descriptions – memory support functions (Continued)

Pad #	Pad name and/or function	Pad name or alt function	Pad voltage	Pad type	Functional description
T28	EBI0_PCCK0		P1	B	PCDDR3 block 1, channel 0 differential clock 0 (+)
T27	EBI0_PCCK0B		P1	B	PCDDR3 block 1, channel 0 differential clock 0 (-)
P27	EBI0_PCCK1B		P1	B	PCDDR3 block 1, channel 0 differential clock 1 (-)
R28	EBI0_PCCKE0		P1	B	PCDDR3 block 1, channel 0 clock enable bit 0
R27	EBI0_PCCKE1		P1	B	PCDDR3 block 1, channel 0 clock enable bit 1
N28	EBI0_PCCS0N		P1	B	PCDDR3 block 1, channel 0 chip select bit 0
N27	EBI0_PCCS1N		P1	B	PCDDR3 block 1, channel 0 chip select bit 1
Y23	EBI0_PCDM0		P1	B	PCDDR3 block 1, channel 0 data mask bit 0
J28	EBI0_PCDM1		P1	B	PCDDR3 block 1, channel 0 data mask bit 1
Y27	EBI0_PCDM2		P1	B	PCDDR3 block 1, channel 0 data mask bit 2
J23	EBI0_PCDM3		P1	B	PCDDR3 block 1, channel 0 data mask bit 3
AC25	EBI0_PCDQ0		P1	B	PCDDR3 block 1, channel 0 data bit 0
AB26	EBI0_PCDQ1		P1	B	PCDDR3 block 1, channel 0 data bit 1
AB25	EBI0_PCDQ2		P1	B	PCDDR3 block 1, channel 0 data bit 2
AB24	EBI0_PCDQ3		P1	B	PCDDR3 block 1, channel 0 data bit 3
AA23	EBI0_PCDQ4		P1	B	PCDDR3 block 1 channel 0 data bit 4
Y25	EBI0_PCDQ5		P1	B	PCDDR3 block 1 channel 0 data bit 5
AA24	EBI0_PCDQ6		P1	B	PCDDR3 block 1 channel 0 data bit 6
Y24	EBI0_PCDQ7		P1	B	PCDDR3 block 1 channel 0 data bit 7
J27	EBI0_PCDQ8		P1	B	PCDDR3 block 1 channel 0 data bit 8
H28	EBI0_PCDQ9		P1	B	PCDDR3 block 1 channel 0 data bit 9
H27	EBI0_PCDQ10		P1	B	PCDDR3 block 1 channel 0 data bit 10
G28	EBI0_PCDQ11		P1	B	PCDDR3 block 1, channel 0 data bit 11
G27	EBI0_PCDQ12		P1	B	PCDDR3 block 1, channel 0 data bit 12
F28	EBI0_PCDQ13		P1	B	PCDDR3 block 1, channel 0 data bit 13
F27	EBI0_PCDQ14		P1	B	PCDDR3 block 1, channel 0 data bit 14
E28	EBI0_PCDQ15		P1	B	PCDDR3 block 1, channel 0 data bit 15
AD27	EBI0_PCDQ16		P1	B	PCDDR3 block 1, channel 0 data bit 16
AC28	EBI0_PCDQ17		P1	B	PCDDR3 block 1, channel 0 data bit 17
AC27	EBI0_PCDQ18		P1	B	PCDDR3 block 1, channel 0 data bit 18
AB28	EBI0_PCDQ19		P1	B	PCDDR3 block 1, channel 0 data bit 19
AB27	EBI0_PCDQ20		P1	B	PCDDR3 block 1, channel 0 data bit 20
AA28	EBI0_PCDQ21		P1	B	PCDDR3 block 1, channel 0 data bit 21
AA27	EBI0_PCDQ22		P1	B	PCDDR3 block 1, channel 0 data bit 22
Y28	EBI0_PCDQ23		P1	B	PCDDR3 block 1, channel 0 data bit 23
J24	EBI0_PCDQ24		P1	B	PCDDR3 block 1, channel 0 data bit 24
J25	EBI0_PCDQ25		P1	B	PCDDR3 block 1, channel 0 data bit 25
H23	EBI0_PCDQ26		P1	B	PCDDR3 block 1, channel 0 data bit 26
H24	EBI0_PCDQ27		P1	B	PCDDR3 block 1, channel 0 data bit 27
G25	EBI0_PCDQ28		P1	B	PCDDR3 block 1, channel 0 data bit 28

Table 6-6 APQ8064 pin descriptions – memory support functions (Continued)

Pad #	Pad name and/or function	Pad name or alt function	Pad voltage	Pad type	Functional description
G26	EBI0_PCDQ29		P1	B	PCDDR3 block 1, channel 0 data bit 29
G24	EBI0_PCDQ30		P1	B	PCDDR3 block 1, channel 0 data bit 30
F25	EBI0_PCDQ31		P1	B	PCDDR3 block 1, channel 0 data bit 31
V25	EBI0_PCDQS0		P1	B	PCDDR3 block 1, channel 0 differential data strobe for byte 0 (+)
V26	EBI0_PCDQSB0		P1	B	PCDDR3 block 1, channel 0 differential data strobe for byte 0 (-)
K28	EBI0_PCDQS1		P1	B	PCDDR3 block 1, channel 0 differential data strobe for byte 1 (+)
K27	EBI0_PCDQSB1		P1	B	PCDDR3 block 1, channel 0 differential data strobe for byte 1 (-)
W28	EBI0_PCDQS2		P1	B	PCDDR3 block 1, channel 0 differential data strobe for byte 2 (+)
W27	EBI0_PCDQSB2		P1	B	PCDDR3 block 1, channel 0 differential data strobe for byte 2 (-)
L26	EBI0_PCDQS3		P1	B	PCDDR3 block 1, channel 0 differential data strobe for byte 3 (+)
L25	EBI0_PCDQSB3		P1	B	PCDDR3 block 1, channel 0 differential data strobe for byte 3 (-)
P28	EBI0_PCK1		P1	B	PCDDR3 block 1, channel 0 differential clock (+)
M28	EBI0_PCODT0		P1	B	PCDDR3 block 1, channel 0 ODT bit 0
V28	EBI0_PCODT1		P1	B	PCDDR3 block 1, channel 0 ODT bit 1
L27	EBI0_PCRASN		P1	B	PCDDR3 block 1, channel 0 RAS
L22	EBI0_PCRSTN		P1	B	PCDDR3 block 1, channel 0 reset
M27	EBI0_PCWEN		P1	B	PCDDR3 block 1, channel 0 write enable
EBI1 for PCDDR3 SDRAM block 1, channel 1					
E17	EBI1_PCA0		P1	DO	PCDDR3 block 1, channel 1 command/address bit 0
F18	EBI1_PCA1		P1	DO	PCDDR3 block 1, channel 1 command/address bit 1
D16	EBI1_PCA2		P1	DO	PCDDR3 block 1, channel 1 command/address bit 2
E16	EBI1_PCA3		P1	DO	PCDDR3 block 1, channel 1 command/address bit 3
F16	EBI1_PCA4		P1	DO	PCDDR3 block 1, channel 1 command/address bit 4
E13	EBI1_PCA5		P1	DO	PCDDR3 block 1, channel 1 command/address bit 5
F13	EBI1_PCA6		P1	DO	PCDDR3 block 1, channel 1 command/address bit 6
D13	EBI1_PCA7		P1	DO	PCDDR3 block 1, channel 1 command/address bit 7
E12	EBI1_PCA8		P1	DO	PCDDR3 block 1, channel 1 command/address bit 8
F11	EBI1_PCA9		P1	DO	PCDDR3 block 1, channel 1 command/address bit 9
G14	EBI1_PCA10		P1	B	PCDDR3 block 1, channel 1 command/address bit 10
F14	EBI1_PCA11		P1	B	PCDDR3 block 1, channel 1 command/address bit 11
F15	EBI1_PCA12		P1	B	PCDDR3 block 1, channel 1 command/address bit 12
G15	EBI1_PCA13		P1	B	PCDDR3 block 1, channel 1 command/address bit 13
G18	EBI1_PCA14		P1	B	PCDDR3 block 1, channel 1 command/address bit 14
B17	EBI1_PCBA0		P1	B	PCDDR3 block 1, channel 1 byte access bit 0
B18	EBI1_PCBA1		P1	B	PCDDR3 block 1, channel 1 byte access bit 1
A17	EBI1_PCBA2		P1	B	PCDDR3 block 1, channel 1 byte access bit 2
J11	EBI1_PCCAL		P1	B	PCDDR3 block 1, channel 1 I/O calibration pad
A11	EBI1_PCCASN		P1	B	PCDDR3 block 1, channel 1 CAS
A16	EBI1_PCCK0		P1	B	PCDDR3 block 1, channel 1 differential clock 0 (+)
B16	EBI1_PCCK0B		P1	B	PCDDR3 block 1, channel 1 differential clock 0 (-)

Table 6-6 APQ8064 pin descriptions – memory support functions (Continued)

Pad #	Pad name and/or function	Pad name or alt function	Pad voltage	Pad type	Functional description
B14	EBI1_PCCK1B		P1	B	PCDDR3 block 1, channel 1 differential clock 1 (-)
A15	EBI1_PCCKE0		P1	B	PCDDR3 block 1, channel 1 clock enable bit 0
B15	EBI1_PCCKE1		P1	B	PCDDR3 block 1, channel 1 clock enable bit 1
A13	EBI1_PCCS0N		P1	B	PCDDR3 block 1, channel 1 chip select bit 0
B13	EBI1_PCCS1N		P1	B	PCDDR3 block 1, channel 1 chip select bit 1
F20	EBI1_PCDM0		P1	B	PCDDR3 block 1, channel 1 data mask bit 0
A9	EBI1_PCDM1		P1	B	PCDDR3 block 1, channel 1 data mask bit 1
B20	EBI1_PCDM2		P1	B	PCDDR3 block 1, channel 1 data mask bit 2
F9	EBI1_PCDM3		P1	B	PCDDR3 block 1, channel 1 data mask bit 3
D23	EBI1_PCDQ0		P1	B	PCDDR3 block 1, channel 1 data bit 0
C22	EBI1_PCDQ1		P1	B	PCDDR3 block 1, channel 1 data bit 1
D22	EBI1_PCDQ2		P1	B	PCDDR3 block 1, channel 1 data bit 2
E22	EBI1_PCDQ3		P1	B	PCDDR3 block 1, channel 1 data bit 3
F21	EBI1_PCDQ4		P1	B	PCDDR3 block 1, channel 1 data bit 4
D20	EBI1_PCDQ5		P1	B	PCDDR3 block 1, channel 1 data bit 5
E21	EBI1_PCDQ6		P1	B	PCDDR3 block 1, channel 1 data bit 6
E20	EBI1_PCDQ7		P1	B	PCDDR3 block 1, channel 1 data bit 7
B9	EBI1_PCDQ8		P1	B	PCDDR3 block 1, channel 1 data bit 8
A8	EBI1_PCDQ9		P1	B	PCDDR3 block 1, channel 1 data bit 9
B8	EBI1_PCDQ10		P1	B	PCDDR3 block 1, channel 1 data bit 10
A7	EBI1_PCDQ11		P1	B	PCDDR3 block 1, channel 1 data bit 11
B7	EBI1_PCDQ12		P1	B	PCDDR3 block 1, channel 1 data bit 12
A6	EBI1_PCDQ13		P1	B	PCDDR3 block 1, channel 1 data bit 13
B6	EBI1_PCDQ14		P1	B	PCDDR3 block 1, channel 1 data bit 14
A5	EBI1_PCDQ15		P1	B	PCDDR3 block 1, channel 1 data bit 15
B24	EBI1_PCDQ16		P1	B	PCDDR3 block 1, channel 1 data bit 16
A23	EBI1_PCDQ17		P1	B	PCDDR3 block 1, channel 1 data bit 17
B23	EBI1_PCDQ18		P1	B	PCDDR3 block 1, channel 1 data bit 18
A22	EBI1_PCDQ19		P1	B	PCDDR3 block 1, channel 1 data bit 19
B22	EBI1_PCDQ20		P1	B	PCDDR3 block 1, channel 1 data bit 20
A21	EBI1_PCDQ21		P1	B	PCDDR3 block 1, channel 1 data bit 21
B21	EBI1_PCDQ22		P1	B	PCDDR3 block 1, channel 1 data bit 22
A20	EBI1_PCDQ23		P1	B	PCDDR3 block 1, channel 1 data bit 23
E9	EBI1_PCDQ24		P1	B	PCDDR3 block 1, channel 1 data bit 24
D9	EBI1_PCDQ25		P1	B	PCDDR3 block 1, channel 1 data bit 25
F8	EBI1_PCDQ26		P1	B	PCDDR3 block 1, channel 1 data bit 26
E8	EBI1_PCDQ27		P1	B	PCDDR3 block 1, channel 1 data bit 27
D7	EBI1_PCDQ28		P1	B	PCDDR3 block 1, channel 1 data bit 28
C7	EBI1_PCDQ29		P1	B	PCDDR3 block 1, channel 1 data bit 29
E7	EBI1_PCDQ30		P1	B	PCDDR3 block 1, channel 1 data bit 30

Table 6-6 APQ8064 pin descriptions – memory support functions (Continued)

Pad #	Pad name and/or function	Pad name or alt function	Pad voltage	Pad type	Functional description
D6	EBI1_PCDQ31		P1	B	PCDDR3 block 1, channel 1 data bit 31
D18	EBI1_PCDQS0		P1	B	PCDDR3 block 1, channel 1 differential data strobe for byte 0 (+)
C18	EBI1_PCDQSB0		P1	B	PCDDR3 block 1, channel 1 differential data strobe for byte 0 (-)
A10	EBI1_PCDQS1		P1	B	PCDDR3 block 1, channel 1 differential data strobe for byte 1 (+)
B10	EBI1_PCDQSB1		P1	B	PCDDR3 block 1, channel 1 differential data strobe for byte 1 (-)
A19	EBI1_PCDQS2		P1	B	PCDDR3 block 1, channel 1 differential data strobe for byte 2 (+)
B19	EBI1_PCDQSB2		P1	B	PCDDR3 block 1, channel 1 differential data strobe for byte 2 (-)
C11	EBI1_PCDQS3		P1	B	PCDDR3 block 1, channel 1 differential data strobe for byte 3 (+)
D11	EBI1_PCDQSB3		P1	B	PCDDR3 block 1, channel 1 differential data strobe for byte 3 (-)
A14	EBI1_PCK1		P1	B	PCDDR3 block 1, channel 1 differential clock (+)
A12	EBI1_PCODT0		P1	B	PCDDR3 block 1, channel 1 ODT bit 0
A18	EBI1_PCODT1		P1	B	PCDDR3 block 1, channel 1 ODT bit 1
B11	EBI1_PCRASN		P1	B	PCDDR3 block 1, channel 1 RAS
G11	EBI1_PCRSTN		P1	B	PCDDR3 block 1, channel 1 reset
B12	EBI1_PCWEN		P1	B	PCDDR3 block 1, channel 1 write enable

Table 6-7 APQ8064 pin descriptions – multimedia functions [a]

Pad #	Pad name and/or function	Pad name or alt function	Pad voltage	Pad type	Functional description
Primary camera serial interface – 4-lane MIPI-CSI (CSI0)					
AH5	MIPI_CSI0_CLK_P		–	AI	MIPI camera serial interface 0 clock – positive
AG5	MIPI_CSI0_CLK_N		–	AI	MIPI camera serial interface 0 clock – negative
AH6	MIPI_CSI0_LN3_P		–	AI, AO	MIPI camera serial interface 0 lane 3 – positive
AG6	MIPI_CSI0_LN3_N		–	AI, AO	MIPI camera serial interface 0 lane 3 – negative
AF6	MIPI_CSI0_LN2_P		–	AI, AO	MIPI camera serial interface 0 lane 2 – positive
AE6	MIPI_CSI0_LN2_N		–	AI, AO	MIPI camera serial interface 0 lane 2 – negative
AF5	MIPI_CSI0_LN1_P		–	AI, AO	MIPI camera serial interface 0 lane 1 – positive
AE5	MIPI_CSI0_LN1_N		–	AI, AO	MIPI camera serial interface 0 lane 1 – negative
AD5	MIPI_CSI0_LN0_P		–	AI, AO	MIPI camera serial interface 0 lane 0 – positive
AE4	MIPI_CSI0_LN0_N		–	AI, AO	MIPI camera serial interface 0 lane 0 – negative
Secondary camera serial interface – 2-lane MIPI-CSI (CSI1)					
AH3	MIPI_CSI1_CLK_P		–	AI	MIPI camera serial interface 1 clock – positive
AG3	MIPI_CSI1_CLK_N		–	AI	MIPI camera serial interface 1 clock – negative
AF2	MIPI_CSI1_LN1_P		–	AI, AO	MIPI camera serial interface 1 lane 1 – positive
AF1	MIPI_CSI1_LN1_N		–	AI, AO	MIPI camera serial interface 1 lane 1 – negative
AH4	MIPI_CSI1_LN0_P		–	AI, AO	MIPI camera serial interface 1 lane 0 – positive
AG4	MIPI_CSI1_LN0_N		–	AI, AO	MIPI camera serial interface 1 lane 0 – negative
3D camera serial interface – 1-lane MIPI-CSI (CSI2) [b]					
AF6	MIPI_CSI2_CLK_P		–	AI	MIPI camera serial interface 2 clock – positive
AE6	MIPI_CSI2_CLK_N		–	AI	MIPI camera serial interface 2 clock – negative

Table 6-7 APQ8064 pin descriptions – multimedia functions [a] (Continued)

Pad #	Pad name and/or function	Pad name or alt function	Pad voltage	Pad type	Functional description
AF5	MIPI_CSI2_LN0_P		–	AI, AO	MIPI camera serial interface 2 lane 0 – positive
AE5	MIPI_CSI2_LN0_N		–	AI, AO	MIPI camera serial interface 2 lane 0 – negative
Camera-related timing signals					
AG23	CAM_MCLK2	GPIO_2	P3	DO B-PD:nppukp	Camera master clock 2 Configurable I/O
AG24	CAM_MCLK1	GPIO_4	P3	DO B-PD:nppukp	Camera master clock 1 Configurable I/O
AG25	CAM_MCLK0	GPIO_5	P3	DO B-PD:nppukp	Camera master clock 0 Configurable I/O
AF25	VFE_CAM_TIMER_7C	GPIO_11	P3	DO BH-PD:nppukp	VFE camera I/F timer 7C; sync or async configurable Configurable I/O
F7	VFE_CAM_TIMER_7B	GPIO_1	P3	DO B-PD:nppukp	VFE camera I/F timer 7B; sync or async configurable Configurable I/O
V7	VFE_CAM_TIMER_7A	GPIO_47	P3	DO BH-PD:nppukp	VFE camera I/F timer 7A; sync or async configurable Configurable I/O
AD26	VFE_CAM_TIMER_6C	GPIO_10	P3	DO BH-PD:nppukp	VFE camera I/F timer 6C; sync or async configurable Configurable I/O
E6	VFE_CAM_TIMER_6B	GPIO_0	P3	DO B-PD:nppukp	VFE camera I/F timer 6B; sync or async configurable Configurable I/O
V4	VFE_CAM_TIMER_6A	GPIO_51	P3	DO B-PD:nppukp	VFE camera I/F timer 6A; sync or async configurable Configurable I/O
AF27	VFE_CAM_TIMER_5B	GPIO_19	P3	DO BH-PD:nppukp	VFE camera I/F timer 5B; sync or async configurable Configurable I/O
AB5	VFE_CAM_TIMER_5A	GPIO_46	P3	DO B-PD:nppukp	VFE camera I/F timer 5A; sync or async configurable Configurable I/O
AC24	VFE_CAM_TIMER_4C	GPIO_6	P3	DO BH-PD:nppukp	VFE camera I/F timer 4C; sync or async configurable Configurable I/O
H15	VFE_CAM_TIMER_4B	GPIO_88	P4	DO BH-PD:nppukp	VFE camera I/F timer 4B; sync or async configurable Configurable I/O
AA5	VFE_CAM_TIMER_4A	GPIO_45	P3	DO BH-PD:nppukp	VFE camera I/F timer 4A; sync or async configurable Configurable I/O
H17	VFE_CAM_TIMER_3B	GPIO_89	P4	DO B-PD:nppukp	VFE camera I/F timer 3B; sync or async configurable Configurable I/O
AG24	VFE_CAM_TIMER_3A	GPIO_4	P3	DO B-PD:nppukp	VFE camera I/F timer 3A; sync or async configurable Configurable I/O
AE22	VFE_CAM_TIMER_2	GPIO_3	P3	DO B-PD:nppukp	VFE camera I/F timer 2; sync or async configurable Configurable I/O
AA20	VFE_CAM_TIMER_1B	GPIO_18	P3	DO BH-PD:nppukp	VFE camera I/F timer 1B; sync or async configurable Configurable I/O
AG23	VFE_CAM_TIMER_1A	GPIO_2	P3	DO B-PD:nppukp	VFE camera I/F timer 1A; sync or async configurable Configurable I/O
Mobile display processor (MDP) vertical sync					
AF25	MDP_VSYNC_E	GPIO_11	P3	B BH-PD:nppukp	MDP vertical sync – external Configurable I/O
E6	MDP_VSYNC_P	GPIO_0	P3	B B-PD:nppukp	MDP vertical sync – primary Configurable I/O

Table 6-7 APQ8064 pin descriptions – multimedia functions [a] (Continued)

Pad #	Pad name and/or function	Pad name or alt function	Pad voltage	Pad type	Functional description
F7	MDP_VSYNC_S	GPIO_1	P3	B B-PD:nppukp	MDP vertical sync – secondary Configurable I/O
Primary display serial interface – 4-lane MIPI-DSI (DSI0)					
AH9	MIPI_DSI0_CLK_P		–	AO	MIPI display serial interface 0 clock – positive
AG9	MIPI_DSI0_CLK_N		–	AO	MIPI display serial interface 0 clock – negative
AD9	MIPI_DSI0_LN3_P		–	AI, AO	MIPI display serial interface 0 lane 3 – positive
AC9	MIPI_DSI0_LN3_N		–	AI, AO	MIPI display serial interface 0 lane 3 – negative
AB7	MIPI_DSI0_LN2_P		–	AI, AO	MIPI display serial interface 0 lane 2 – positive
AB9	MIPI_DSI0_LN2_N		–	AI, AO	MIPI display serial interface 0 lane 2 – negative
AH10	MIPI_DSI0_LN1_P		–	AI, AO	MIPI display serial interface 0 lane 1 – positive
AG10	MIPI_DSI0_LN1_N		–	AI, AO	MIPI display serial interface 0 lane 1 – negative
AF9	MIPI_DSI0_LN0_P		–	AI, AO	MIPI display serial interface 0 lane 0 – positive
AE9	MIPI_DSI0_LN0_N		–	AI, AO	MIPI display serial interface 0 lane 0 – negative
Y9	MIPI_DSI_CAL		–	AI, AO	MIPI display serial interface 0 & 1 calibration
Y10	MIPI_DSI_LDO		–	AI, AO	MIPI display serial interface 0 & 1 low dropout regulator
Secondary display serial interface – 4-lane MIPI-DSI (DSI1)					
AH8	MIPI_DSI1_CLK_P		–	AI	MIPI display serial interface 1 clock – positive
AG8	MIPI_DSI1_CLK_N		–	AI	MIPI display serial interface 1 clock – negative
AF7	MIPI_DSI1_LN3_P		–	AI, AO	MIPI display serial interface 1 lane 3 – positive
AE7	MIPI_DSI1_LN3_N		–	AI, AO	MIPI display serial interface 1 lane 3 – negative
AH7	MIPI_DSI1_LN2_P		–	AI, AO	MIPI display serial interface 1 lane 2 – positive
AG7	MIPI_DSI1_LN2_N		–	AI, AO	MIPI display serial interface 1 lane 2 – negative
AD7	MIPI_DSI1_LN1_P		–	AI, AO	MIPI display serial interface 1 lane 1 – positive
AC7	MIPI_DSI1_LN1_N		–	AI, AO	MIPI display serial interface 1 lane 1 – negative
AD8	MIPI_DSI1_LN0_P		–	AI, AO	MIPI display serial interface 1 lane 0 – positive
AC8	MIPI_DSI1_LN0_N		–	AI, AO	MIPI display serial interface 1 lane 0 – negative
Y9	MIPI_DSI_CAL		–	AI, AO	MIPI display serial interface 0 & 1 calibration
Y10	MIPI_DSI_LDO		–	AI, AO	MIPI display serial interface 0 & 1 low dropout regulator
High-definition multimedia interface (HDMI)					
AH14	HDMI_TCLK_P		–	AO	HDMI differential clock – plus
AG14	HDMI_TCLK_M		–	AO	HDMI differential clock – minus
AB15	HDMI_TX2_P		–	AO	HDMI differential transmit 2 – plus
AC15	HDMI_TX2_M		–	AO	HDMI differential transmit 2 – minus
AH15	HDMI_TX1_P		–	AO	HDMI differential transmit 1 – plus
AG15	HDMI_TX1_M		–	AO	HDMI differential transmit 1 – minus
AB14	HDMI_TX0_P		–	AO	HDMI differential transmit 0 – plus
AA14	HDMI_TX0_M		–	AO	HDMI differential transmit 0 – minus
AA13	HDMI_REXT		–	AI, AO	HDMI external calibration resistor
A3	HDMI_CEC	GPIO_69	P3	B B-PU:nppdkp	HDMI consumer electronics control Configurable I/O

Table 6-7 APQ8064 pin descriptions – multimedia functions [a] (Continued)

Pad #	Pad name and/or function	Pad name or alt function	Pad voltage	Pad type	Functional description
C4	HDMI_DDC_CLK	GPIO70	P3	B B-PU:nppdkp	HDMI display data channel – clock Configurable I/O
A4	HDMI_DDC_DATA	GPIO_71	P3	B B-PU:nppdkp	HDMI display data channel – data Configurable I/O
H12	HDMI_HPLUG_DET	GPIO_72	P3	DI BH-PD:nppukp	HDMI hot plug detect Configurable I/O
Alternate primary display interface - low-voltage differential signaling (LVDS) interface					
AH12	LVDS_CLK1_P		P3	DO	LVDS clock 1 – plus
AG12	LVDS_CLK1_M		P3	DO	LVDS clock 1 – minus
AG11	LVDS_CLK0_P		P3	DO	LVDS clock 0 – plus
AH11	LVDS_CLK0_M		P3	DO	LVDS clock 0 – minus
AG13	LVDS_TX7_P		P3	DO	LVDS differential transmit 7 – plus
AH13	LVDS_TX7_M		P3	DO	LVDS differential transmit 7 – minus
AE13	LVDS_TX6_P		P3	DO	LVDS differential transmit 6 – plus
AF13	LVDS_TX6_M		P3	DO	LVDS differential transmit 6 – minus
AC13	LVDS_TX5_P		P3	DO	LVDS differential transmit 5 – plus
AD13	LVDS_TX5_M		P3	DO	LVDS differential transmit 5 – minus
AB13	LVDS_TX4_P		P3	DO	LVDS differential transmit 4 – plus
AC14	LVDS_TX4_M		P3	DO	LVDS differential transmit 4 – minus
AF11	LVDS_TX3_P		P3	DO	LVDS differential transmit 3 – plus
AE11	LVDS_TX3_M		P3	DO	LVDS differential transmit 3 – minus
AD12	LVDS_TX2_P		P3	DO	LVDS differential transmit 2 – plus
AC11	LVDS_TX2_M		P3	DO	LVDS differential transmit 2 – minus
AA12	LVDS_TX1_P		P3	DO	LVDS differential transmit 1 – plus
Y12	LVDS_TX1_M		P3	DO	LVDS differential transmit 1 – minus
AA11	LVDS_TX0_P		P3	DO	LVDS differential transmit 0 – plus
Y11	LVDS_TX0_M		P3	DO	LVDS differential transmit 0 – minus
Also see Table 6-8 for connectivity ports that are used for multimedia applications: Audio – I^2S, MI^2S, SLIMbus, PCM; controls – I^2C					

a. Refer to Table 6-5 for parameter and acronym definitions.
b. MIPI_CSI2 is muxed behind MIPI_CSI0 for 3D camera usage.

NOTE GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the table above), designers must identify all their application's requirements and map each GPIO to its function – carefully avoiding conflicts in GPIO assignments. Refer to Chapter 11 – GPIO for a list of all supported functions for each GPIO.

Table 6-8 APQ8064 pin descriptions – connectivity functions [a]

Pad #	Pad name and/or function	Pad name or alt function	Pad voltage	Pad type	Functional description
Audio I²S interface – primary speaker					
AD3	CDC_SPKR_I2S_DOUT	GPIO_41	P3	DO BH-PD:nppukp	Primary speaker codec I²S data output Configurable I/O
AD2	CDC_SPKR_I2S_SCK	GPIO_40	P3	B B-PD:nppukp	Primary speaker codec I²S bit clock Configurable I/O
V6	CDC_SPKR_I2S_WS	GPIO_42	P3	B BH-PD:nppukp	Primary speaker codec I²S word select (L/R) Configurable I/O
AA6	CDC_SPKR_I2S_MCLK	GPIO_39	P3	DO BH-PD:nppukp	Primary speaker codec I²S master clock Configurable I/O
Audio I²S interface – secondary speaker					
W2	SPKR_I2S_DOUT	GPIO_49	P3	DO BH-PD:nppukp	Secondary speaker codec I²S data output Configurable I/O
V7	SPKR_I2S_SCK	GPIO_47	P3	B BH-PD:nppukp	Secondary speaker codec I²S bit clock Configurable I/O
V1	SPKR_I2S_WS	GPIO_48	P3	B B-PD:nppukp	Secondary speaker codec I²S word select (L/R) Configurable I/O
V3	SPKR_I2S_MCLK	GPIO_50	P3	DO BH-PD:nppukp	Secondary speaker codec I²S master clock Configurable I/O
Audio MI²S interface – 8-channel (7.1 speaker, 5.1 microphone)					
Y3	MI2S_SD3	GPIO_29	P3	B BH-PD:nppukp	Multiple I²S interface serial data channel 3 Configurable I/O
AC1	MI2S_SD2	GPIO_30	P3	B BH-PD:nppukp	Multiple I²S interface serial data channel 2 Configurable I/O
AD1	MI2S_SD1	GPIO_31	P3	B B-PD:nppukp	Multiple I²S interface serial data channel 1 Configurable I/O
Y1	MI2S_SD0	GPIO_32	P3	B BH-PD:nppukp	Multiple I²S interface serial data channel 0 Configurable I/O
Y6	MI2S_SCK	GPIO_28	P3	B B-PD:nppukp	Multiple I²S interface bit clock Configurable I/O
AA2	MI2S_WS	GPIO_27	P3	B B-PD:nppukp	Multiple I²S interface word select (L/R) Configurable I/O
AA1	MI2S_MCLK	GPIO_33	P3	DO B-PD:nppukp	Multiple I²S interface master clock Configurable I/O
Audio I²S interface – primary microphone (quad mic support)					
B4	CDC_MIC_I2S_DIN1	GPIO_38	P3	DI BH-PD:nppukp	Primary microphone codec I²S data input 1 Configurable I/O
E5	CDC_MIC_I2S_DIN0	GPIO_37	P3	DI B-PD:nppukp	Primary microphone codec I²S data input 0 Configurable I/O
H10	CDC_MIC_I2S_SCK	GPIO_35	P3	B B-PD:nppukp	Primary microphone codec I²S bit clock Configurable I/O
B5	CDC_MIC_I2S_WS	GPIO_36	P3	B BH-PD:nppukp	Primary microphone codec I²S word select (L/R) Configurable I/O
B3	CDC_MIC_I2S_MCLK	GPIO_34	P3	DO BH-PD:nppukp	Primary microphone codec I²S master clock Configurable I/O

Table 6-8 APQ8064 pin descriptions – connectivity functions [a] (Continued)

Pad #	Pad name and/or function	Pad name or alt function	Pad voltage	Pad type	Functional description
Audio I²S interface – secondary microphone					
V4	MIC_I2S_DIN	GPIO_51	P3	DI B-PD:nppukp	Secondary microphone codec I²S data input Configurable I/O
V5	MIC_I2S_SCK	GPIO_52	P3	B BH-PD:nppukp	Secondary microphone codec I²S bit clock Configurable I/O
U1	MIC_I2S_WS	GPIO_53	P3	B B-PD:nppukp	Secondary microphone codec I²S word select (L/R) Configurable I/O
U2	MIC_I2S_MCLK	GPIO_54	P3	DO B-PD:nppukp	Secondary microphone codec I²S master clock Configurable I/O
Audio PCM interface					
AB1	AUDIO_PCM_DIN	GPIO_44	P3	DI BH-PD:nppukp	Audio PCM data input Configurable I/O
W1	AUDIO_PCM_DOUT	GPIO_43	P3	DO-Z B-PD:nppukp	Audio PCM data output Configurable I/O
AB5	AUDIO_PCM_CLK	GPIO_46	P3	B B-PD:nppukp	Audio PCM clock Configurable I/O
AA5	AUDIO_PCM_SYNC	GPIO_45	P3	B BH-PD:nppukp	Audio PCM sync Configurable I/O
Audio SLIMbus – bidirectional multiplexed audio					
AD3	AUD_SB1_DATA_A	GPIO_41	P3	B BH-PD:nppukp	Audio bidirectional data (A) via SLIMbus 1 Configurable I/O
AC1	AUD_SB1_DATA_B	GPIO_30	P3	B BH-PD:nppukp	Audio bidirectional data (B) via SLIMbus 1 Configurable I/O
AD2	AUD_SB1_CLK_A	GPIO_40	P3	B B-PD:nppukp	Audio clock (A) for SLIMbus 1 Configurable I/O
AD1	AUD_SB1_CLK_B	GPIO_31	P3	B B-PD:nppukp	Audio clock (B) for SLIMbus 1 Configurable I/O
AA6	AUD_SB1_MCLK	GPIO_39	P3	DO BH-PD:nppukp	Audio master clock for SLIMbus 1 Configurable I/O
Secure digital controller 1 (SDC1) interface – supports eMMC NAND					
A26	SDC1_DATA_7		P3	B	Secure digital controller 1 data bit 7
A25	SDC1_DATA_6		P3	B	Secure digital controller 1 data bit 6
C25	SDC1_DATA_5		P3	B	Secure digital controller 1 data bit 5
E24	SDC1_DATA_4		P3	B	Secure digital controller 1 data bit 4
B26	SDC1_DATA_3		P3	B	Secure digital controller 1 data bit 3
A24	SDC1_DATA_2		P3	B	Secure digital controller 1 data bit 2
B25	SDC1_DATA_1		P3	B	Secure digital controller 1 data bit 1
E23	SDC1_DATA_0		P3	B	Secure digital controller 1 data bit 0
D24	SDC1_CMD		P3	B	Secure digital controller 1 command
C24	SDC1_CLK		P3	DO	Secure digital controller 1 clock
Secure digital controller 2 (SDC2) interface					
G6	SDC2_DATA_3	GPIO_58	P3	B BH-PD:nppukp	Secure digital controller 2 data bit 3 Configurable I/O

Table 6-8 APQ8064 pin descriptions – connectivity functions [a] (Continued)

Pad #	Pad name and/or function	Pad name or alt function	Pad voltage	Pad type	Functional description
H8	SDC2_DATA_2	GPIO_60	P3	B B-PD:nppukp	Secure digital controller 2 data bit 2 Configurable I/O
C6	SDC2_DATA_1	GPIO_61	P3	B BH-PD:nppukp	Secure digital controller 2 data bit 1 Configurable I/O
D1	SDC2_DATA_0	GPIO_62	P3	B B-PD:nppukp	Secure digital controller 2 data bit 0 Configurable I/O
E1	SDC2_CMD	GPIO_57	P3	B B-PD:nppukp	Secure digital controller 2 command Configurable I/O
H5	SDC2_CLK	GPIO_59	P3	DO B-PD:nppukp	Secure digital controller 2 clock Configurable I/O
Secure digital controller 3 (SDC3) interface					
F1	SDC3_DATA_3		P2	B	Secure digital controller 3 data bit 3 (dual voltage)
G1	SDC3_DATA_2		P2	B	Secure digital controller 3 data bit 2 (dual voltage)
F2	SDC3_DATA_1		P2	B	Secure digital controller 3 data bit 1 (dual voltage)
G2	SDC3_DATA_0		P2	B	Secure digital controller 3 data bit 0 (dual voltage)
H2	SDC3_CMD		P2	B	Secure digital controller 3 command (dual voltage)
G3	SDC3_CLK		P2	DO	Secure digital controller 3 clock (dual voltage)
Secure digital controller 4 (SDC4) interface					
AC2	SDC4_DATA_3	GPIO_63	P3	B BH-PD:nppukp	Secure digital controller 4 data bit 3 Configurable I/O
AB4	SDC4_DATA_2	GPIO_64	P3	B B-PD:nppukp	Secure digital controller 4 data bit 2 Configurable I/O
AB2	SDC4_DATA_1	GPIO_65	P3	B BH-PD:nppukp	Secure digital controller 4 data bit 1 Configurable I/O
AB3	SDC4_DATA_0	GPIO_66	P3	B B-PD:nppukp	Secure digital controller 4 data bit 0 Configurable I/O
AC3	SDC4_CMD	GPIO_67	P3	B B-PD:nppukp	Secure digital controller 4 command Configurable I/O
Y2	SDC4_CLK	GPIO_68	P3	DO B-PD:nppukp	Secure digital controller 4 clock Configurable I/O
Serial peripheral interface (SPI) extra chip selects (supplements GSBI ports configured for SPI protocol)					
AE26	SPI_CS1A_N_GSBI1	GPIO_7	P3	DO-Z BH-PD:nppukp	Serial peripheral interface chip-select 1A for SPI on GSBI1 Configurable I/O
AD26	SPI_CS1B_N_GSBI1	GPIO_10	P3	DO-Z BH-PD:nppukp	Serial peripheral interface chip-select 1B for SPI on GSBI1 Configurable I/O
B5	SPI_CS1C_N_GSBI1	GPIO_36	P3	DO-Z BH-PD:nppukp	Serial peripheral interface chip-select 1C for SPI on GSBI1 Configurable I/O
AC24	SPI_CS2A_N_GSBI1	GPIO_6	P3	DO-Z BH-PD:nppukp	Serial peripheral interface chip-select 2A for SPI on GSBI1 Configurable I/O
AF25	SPI_CS2B_N_GSBI1	GPIO_11	P3	DO-Z BH-PD:nppukp	Serial peripheral interface chip-select 2B for SPI on GSBI1 Configurable I/O
V1	SPI_CS2C_N_GSBI1	GPIO_48	P3	DO-Z B-PD:nppukp	Serial peripheral interface chip-select 2C for SPI on GSBI1 Configurable I/O
H6	SPI_CS3A_N_GSBI1	GPIO_56	P3	DO-Z BH-PD:nppukp	Serial peripheral interface chip-select 3A for SPI on GSBI1 Configurable I/O

Table 6-8 APQ8064 pin descriptions – connectivity functions [a] (Continued)

Pad #	Pad name and/or function	Pad name or alt function	Pad voltage	Pad type	Functional description
AE26	SPI_CS3B_N_GSBI1	GPIO_7	P3	DO-Z BH-PD:nppukp	Serial peripheral interface chip-select 3B for SPI on GSBI1 Configurable I/O
Touch screen interface					
AF24	TS_PENIRQ_N	GPIO_26	P3	DI BH-PU:nppdkp	Touch screen pen-down interrupt Configurable I/O
AE26	TS_EOC	GPIO_7	P3	DI BH-PD:nppdkp	Touch screen end-of-conversion interrupt Configurable I/O
AC24	SSBI_TS	GPIO_6	P3	B BH-PD:nppdkp	Single-wire serial bus interface for touch screen Configurable I/O
Transport stream interface 1 (TSIF1)					
E1	TSIF1_DATA	GPIO_57	P3	DI B-PD:nppukp	Transport stream interface 1 data Configurable I/O
G5	TSIF1_CLK	GPIO_55	P3	DI BH-PD:nppukp	Transport stream interface 1 clock Configurable I/O
D1	TSIF1_SYNC	GPIO_62	P3	DI B-PD:nppukp	Transport stream interface 1 sync Configurable I/O
H6	TSIF1_EN	GPIO_56	P3	DI BH-PD:nppukp	Transport stream interface 1 enable Configurable I/O
Transport stream interface 2 (TSIF2)					
C6	TSIF2_DATA	GPIO_61	P3	DI BH-PD:nppukp	Transport stream interface 2 data Configurable I/O
H5	TSIF2_CLK	GPIO_59	P3	DI B-PD:nppukp	Transport stream interface 2 clock Configurable I/O
G6	TSIF2_SYNC	GPIO_58	P3	DI BH-PD:nppukp	Transport stream interface 2 sync Configurable I/O
H8	TSIF2_EN	GPIO_60	P3	DI B-PD:nppukp	Transport stream interface 2 enable Configurable I/O
USB UICC interface					
U1	UICC_DP	GPIO_53	P3	B B-PD:nppukp	UICC data plus Configurable I/O
U2	UICC_DM	GPIO_54	P3	B B-PD:nppukp	UICC data minus Configurable I/O
USB HS PHY interface 1 (USB1)					
R1	USB1_HS_DP		–	AI, AO	USB1 HS data plus
R2	USB1_HS_DM		–	AI, AO	USB1 HS data minus
T5	USB1_HS_VBUS		–	AI	USB1 HS bus voltage (5 V)
T4	USB1_HS_ID		–	AI, AO	USB1 HS ID (differentiates between mini A or B plugs)
N3	USB1_3_4_HS_SYSCLK		–	DI	USB1, USB3, and USB4 HS system clock (19.2 MHz)
T3	USB1_HS_REXT		–	AI, AO	USB1 HS external resistor – Kelvin connection
USB HS PHY interface 3 (USB3)					
K1	USB3_HS_DP		–	AI, AO	USB3 HS data plus
K2	USB3_HS_DM		–	AI, AO	USB3 HS data minus
L5	USB3_HS_VBUS		–	AI	USB3 HS bus voltage (5 V)
L4	USB3_HS_ID		–	AI, AO	USB3 HS ID (differentiates between mini A or B plugs)

Table 6-8 APQ8064 pin descriptions – connectivity functions [a] (Continued)

Pad #	Pad name and/or function	Pad name or alt function	Pad voltage	Pad type	Functional description
N3	USB1_3_4_HS_SYSCLK		–	DI	USB1, USB3, and USB4 HS system clock (19.2 MHz)
L7	USB3_HS_REXT		–	AI, AO	USB3 HS external resistor – Kelvin connection
USB HS PHY interface 4 (USB4)					
M1	USB4_HS_DP		–	AI, AO	USB4 HS data plus
M2	USB4_HS_DM		–	AI, AO	USB4 HS data minus
N5	USB4_HS_VBUS		–	AI	USB4 HS bus voltage (5 V)
N4	USB4_HS_ID		–	AI, AO	USB4 HS ID (differentiates between mini A or B plugs)
N3	USB1_3_4_HS_SYSCLK		–	DI	USB1, USB3, and USB4 HS system clock (19.2 MHz)
N1	USB4_HS_REXT		–	AI, AO	USB4 HS external resistor – Kelvin connection
HSIC interface (USB2)					
H15	USB2_HSIC_STROBE	GPIO_88	P4	AI, AO B-PD:nppukp	HSIC strobe configurable I/O
H17	USB2_HSIC_DATA	GPIO_89	P4	AI, AO B-PD: nppukp	HSIC data configurable I/O
H18	USB2_HSIC_CAL		P4	AI, AO	HSIC calibration
PCI Express interface (PCIe)					
AH20	PCI_E_REFCLK_P		–	B	PCIe reference clock – plus
AG20	PCI_E_REFCLK_N		–	B	PCIe reference clock – minus
AH21	PCI_E_HSO_P		–	B	PCIe transmit lane – plus
AG21	PCI_E_HSO_N		–	B	PCIe transmit lane – minus
AH19	PCI_E_HSI_P		–	B	PCIe receive lane – plus
AG19	PCI_E_HSI_N		–	B	PCIe receive lane – minus
AC18	PCI_E_REXT		–	B	PCIe external resistor
AD22	pci_e_pwrflt_n	GPIO_86	P3	DI B-PD:nppukp	PCIe power-fault indication Configurable I/O
AF26	PCI_E_PWREN_N	GPIO_85	P3	DI B-PD:nppukp	PCIe interface signal to power up/down the transceiver Configurable I/O
Y20	PCI_E_PRSNT_2_N	GPIO_84	P3	DO BH-PD:nppukp	PCIe interface power presence detection Configurable I/O
AA21	PCI_E_WAKE_N	GPIO_83	P3	DO BH-PD:nppukp	PCIe interface link reactivation Configurable I/O
Y21	PCI_E_RST_N	GPIO_82	P3	DI B-PD:nppukp	PCIe interface core reset Configurable I/O
Serial ATA interface (SATA)					
AF16	SATA_CLKP		–	DO	SATA clock - plus
AE16	SATA_CLKM		–	DO	SATA clock - minus
AH16	SATA_TXP		–	AO	SATA transmit - plus
AG16	SATA_TXM		–	AO	SATA transmit - minus
AG17	SATA_RXP		–	AI	SATA receive - plus
AH17	SATA_RXM		–	AI	SATA receive - minus
AD16	SATA_REXT		–	AI, AO	SATA external resistor
AD17	SATA_TPA		–	AO	SATA test access point

Table 6-8 APQ8064 pin descriptions – connectivity functions [a] (Continued)

Pad #	Pad name and/or function	Pad name or alt function	Pad voltage	Pad type	Functional description
General serial bus interface 1 – see Table 11-2 for application-specific pin assignments					
AA20	GSBI1_3	GPIO_18	P3	B BH-PD:nppukp	General SBI 1 bit 3; UART, UIM, SPI, or I2C Configurable I/O
AF27	GSBI1_2	GPIO_19	P3	B BH-PD:nppukp	General SBI 1 bit 2; UART, UIM, SPI, or I2C Configurable I/O
AG26	GSBI1_1	GPIO_20	P3	B B-PD:nppukp	General SBI 1 bit 1; UART, UIM, SPI, or I2C Configurable I/O
AF23	GSBI1_0	GPIO_21	P3	B B-PD:nppukp	General SBI 1 bit 0; UART, UIM, SPI, or I2C Configurable I/O
General serial bus interface 2 – see Table 11-2 for application-specific pin assignments					
AE21	GSBI2_3	GPIO_22	P3	B BH-PD:nppukp	General SBI 2 bit 3; UART, UIM, SPI, or I2C Configurable I/O
AD24	GSBI2_2	GPIO_23	P3	B BH-PD:nppukp	General SBI 2 bit 2; UART, UIM, SPI, or I2C Configurable I/O
AC23	GSBI2_1	GPIO_24	P3	B B-PD:nppukp	General SBI 2 bit 1; UART, UIM, SPI, or I2C Configurable I/O
AC22	GSBI2_0	GPIO_25	P3	B B-PD:nppukp	General SBI 2 bit 0; UART, UIM, SPI, or I2C Configurable I/O
General serial bus interface 3 – see Table 11-2 for application-specific pin assignments					
AC24	GSBI3_3	GPIO_6	P3	B BH-PD:nppukp	General SBI 3 bit 3; UART, UIM, SPI, or I2C Configurable I/O
AE26	GSBI3_2	GPIO_7	P3	B BH-PD:nppukp	General SBI 3 bit 2; UART, UIM, SPI, or I2C Configurable I/O
AD21	GSBI3_1	GPIO_8	P3	B B-PD:nppukp	General SBI 3 bit 1; UART, UIM, SPI, or I2C Configurable I/O
AD23	GSBI3_0	GPIO_9	P3	B B-PD:nppukp	General SBI 3 bit 0; UART, UIM, SPI, or I2C Configurable I/O
General serial bus interface 4 – see Table 11-2 for application-specific pin assignments					
AD26	GSBI4_3	GPIO_10	P3	B BH-PD:nppukp	General SBI 4 bit 3; UART, UIM, SPI, or I2C Configurable I/O
AF25	GSBI4_2	GPIO_11	P3	B BH-PD:nppukp	General SBI 4 bit 2; UART, UIM, SPI, or I2C Configurable I/O
AD25	GSBI4_1	GPIO_12	P3	B B-PD:nppukp	General SBI 4 bit 1; UART, UIM, SPI, or I2C Configurable I/O
AF22	GSBI4_0	GPIO_13	P3	B B-PD:nppukp	General SBI 4 bit 0; UART, UIM, SPI, or I2C Configurable I/O
General serial bus interface 5 – see Table 11-2 for application-specific pin assignments					
V4	GSBI5_3	GPIO_51	P3	B B-PD:nppukp	General SBI 5 bit 3; UART, UIM, SPI, or I2C Configurable I/O
V5	GSBI5_2	GPIO_52	P3	B BH-PD:nppukp	General SBI 5 bit 2; UART, UIM, SPI, or I2C Configurable I/O
U1	GSBI5_1	GPIO_53	P3	B B-PD:nppukp	General SBI 5 bit 1; UART, UIM, SPI, or I2C Configurable I/O
U2	GSBI5_0	GPIO_54	P3	B B-PD:nppukp	General SBI 5 bit 0; UART, UIM, SPI, or I2C Configurable I/O

Table 6-8 APQ8064 pin descriptions – connectivity functions [a] (Continued)

Pad #	Pad name and/or function	Pad name or alt function	Pad voltage	Pad type	Functional description
General serial bus interface 6 – see Table 11-2 for application-specific pin assignments					
H9	GSBI6_3	GPIO_14	P3	B B-PD:nppukp	General SBI 6 bit 3; UART, UIM, SPI, or I2C Configurable I/O
F6	GSBI6_2	GPIO_15	P3	B BH-PD:nppukp	General SBI 6 bit 2; UART, UIM, SPI, or I2C Configurable I/O
C3	GSBI6_1	GPIO_16	P3	B B-PD:nppukp	General SBI 6 bit 1; UART, UIM, SPI, or I2C Configurable I/O
D3	GSBI6_0	GPIO_17	P3	B B-PD:nppukp	General SBI 6 bit 0; UART, UIM, SPI, or I2C Configurable I/O
General serial bus interface 7 – see Table 11-2 for application-specific pin assignments					
Y21	GSBI7_3	GPIO_82	P3	B B-PD:nppukp	General SBI 7 bit 3; UART, UIM, SPI, or I2C Configurable I/O
AA21	GSBI7_2	GPIO_83	P3	B BH-PD:nppukp	General SBI 7 bit 2; UART, UIM, SPI, or I2C Configurable I/O
Y20	GSBI7_1	GPIO_84	P3	B BH-PD:nppukp	General SBI 7 bit 1; UART, UIM, SPI, or I2C Configurable I/O
AF26	GSBI7_0	GPIO_85	P3	B B-PD:nppukp	General SBI 7 bit 0; UART, UIM, SPI, or I2C Configurable I/O

a. Refer to Table 6-5 for parameter and acronym definitions.

NOTE GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the table above), designers must identify all their application's requirements and map each GPIO to its function – carefully avoiding conflicts in GPIO assignments. Refer to Chapter 11 – GPIO for a list of all supported functions for each GPIO.

Table 6-9 APQ8064 pin descriptions – internal functions [a]

Pad #	Pad name and/or function	Pad name or alt function	Pad voltage	Pad type	Functional description
Clocks and related signals, resets, and mode controls					
E27	SLEEP_CLK		P3	DI	Sleep clock
E4	CXO		P3	DI	Core crystal oscillator (system clock at 19.2 MHz)
C2	CXO_EN		P3	DO	Dual function: core crystal oscillator enable
W15	PXO_IN		–	AI	Platform crystal oscillator input (24.576 MHz or 27 MHz)
W14	PXO_OUT		–	AO	Platform crystal oscillator output (24.576 MHz or 27 MHz)
Y1	GP_CLK_2A	GPIO_32	P3	DO BH-PD:nppukp	General-purpose clock output 2A Configurable I/O
AC22	GP_CLK_2B	GPIO_25	P3	DO B-PD:nppukp	General-purpose clock output 2B Configurable I/O
AG24	GP_CLK_1A	GPIO_4	P3	DO B-PD:nppukp	General-purpose clock output 1A Configurable I/O
V3	GP_CLK_1B	GPIO_50	P3	DO BH-PD:nppukp	General-purpose clock output 1B Configurable I/O
AE22	GP_CLK_0A	GPIO_3	P3	DO B-PD:nppukp	General-purpose clock output 0A Configurable I/O

Table 6-9 APQ8064 pin descriptions – internal functions [a] (Continued)

Pad #	Pad name and/or function	Pad name or alt function	Pad voltage	Pad type	Functional description
B3	GP_CLK_0B	GPIO_34	P3	DO BH-PD:nppukp	General-purpose clock output 0B Configurable I/O
AG23	GP_MN	GPIO_2	P3	DO B-PD:nppukp	General-purpose M/N:D counter output Configurable I/O
W2	GP_PDM_2A	GPIO_49	P3	DO BH-PD:nppukp	General-purpose PDM output 2A, 12-bit, clocked at XO/4 Configurable I/O
AA1	GP_PDM_2B	GPIO_33	P3	DO B-PD:nppukp	General-purpose PDM output 2B, 12-bit, clocked at XO/4 Configurable I/O
AE21	GP_PDM_1A	GPIO_22	P3	DO BH-PD:nppukp	General-purpose PDM output 1A, 12-bit, clocked at XO/4 Configurable I/O
AB1	GP_PDM_1B	GPIO_44	P3	DO BH-PD:nppukp	General-purpose PDM output 1B, 12-bit, clocked at XO/4 Configurable I/O
B4	GP_PDM_0A	GPIO_38	P3	DO BH-PD:nppukp	General-purpose PDM output 0A, 12-bit, clocked at XO/4 Configurable I/O
AA20	GP_PDM_0B	GPIO_18	P3	DO BH-PD:nppukp	General-purpose PDM output 0B, 12-bit, clocked at XO/4 Configurable I/O
Resets and mode controls – also see the list of APQ8064 pins (Table 6-10) that can wake up the device					
T21	MODE_1		P3	DI	Mode control bit 1
R21	MODE_0		P3	DI	Mode control bit 0
U21	RESIN_N		P3	DI	Reset input
P21	RESOUT_N		P3	DO	Reset output
AE22	WDOG_DISABLE	GPIO_3	P3	DI B-PD:nppukp	Watchdog timer disable input Configurable I/O
AG24	BOOT_CONFIG_6	GPIO_4	P3	DI B-PD:nppukp	Boot configuration bit 6 (depends on security fuse state) Configurable I/O
AG25	BOOT_CONFIG_5	GPIO_5	P3	DI B-PD:nppukp	Boot configuration bit 5 (depends on security fuse state) Configurable I/O
AA1	BOOT_CONFIG_4	GPIO_33	P3	DI B-PD:nppukp	Boot configuration bit 4 (depends on security fuse state) Configurable I/O
B3	BOOT_CONFIG_3	GPIO_34	P3	DI BH-PD:nppukp	Boot configuration bit 3 (depends on security fuse state) Configurable I/O
AA6	BOOT_CONFIG_2	GPIO_39	P3	DI BH-PD:nppukp	Boot configuration bit 2 (depends on security fuse state) Configurable I/O
V3	BOOT_CONFIG_1	GPIO_50	P3	DI BH-PD:nppukp	Boot configuration bit 1 (depends on security fuse state) Configurable I/O
W21	BOOT_CONFIG_0	GPIO_87	P3	DI B-PD:nppukp	Boot configuration bit 0 (depends on security fuse state) Configurable I/O
AG23	BOOT_FROM_ROM	GPIO_2	P3	DI B-PD:nppukp	Boot configuration bit to select boot from ROM option Configurable I/O
JTAG interfaces					
K21	RTCK		P3	DO	JTAG return clock
D26	SRST_N		P3	DI	JTAG reset for debug
L21	TCK		P3	DI	JTAG clock input
F24	TDI		P3	DI	JTAG data input
D28	TDO		P3	DO-Z	JTAG data output

Table 6-9 APQ8064 pin descriptions – internal functions [a] (Continued)

Pad #	Pad name and/or function	Pad name or alt function	Pad voltage	Pad type	Functional description
D25	TMS		P3	DI	JTAG mode select input
D27	TRST_N		P3	DI	JTAG reset

a. Refer to Table 6-5 for parameter and acronym definitions.

NOTE GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the table above), designers must identify all their application's requirements and map each GPIO to its function – carefully avoiding conflicts in GPIO assignments. Refer to Chapter 11 – GPIO for a list of all supported functions for each GPIO.

Table 6-10 APQ8064 wakeup pins[a]

Pad #	Pad name	Pad voltage	Pad type	Functional description
AC24	GPIO_6	P3	BH-PD:nppukp	Configurable I/O
AE26	GPIO_7	P3	BH-PD:nppukp	Configurable I/O
AD26	GPIO_10	P3	BH-PD:nppukp	Configurable I/O
AF25	GPIO_11	P3	BH-PD:nppukp	Configurable I/O
F6	GPIO_15	P3	BH-PD:nppukp	Configurable I/O
AA20	GPIO_18	P3	BH-PD:nppukp	Configurable I/O
AF27	GPIO_19	P3	BH-PD:nppukp	Configurable I/O
AE21	GPIO_22	P3	BH-PD:nppukp	Configurable I/O
AD24	GPIO_23	P3	BH-PD:nppukp	Configurable I/O
AF24	GPIO_26	P3	BH-PU:nppukp	Configurable I/O
Y3	GPIO_29	P3	BH-PD:nppukp	Configurable I/O
AC1	GPIO_30	P3	BH-PD:nppukp	Configurable I/O
Y1	GPIO_32	P3	BH-PD:nppukp	Configurable I/O
B3	GPIO_34	P3	BH-PD:nppukp	Configurable I/O
B5	GPIO_36	P3	BH-PD:nppukp	Configurable I/O
B4	GPIO_38	P3	BH-PD:nppukp	Configurable I/O
AA6	GPIO_39	P3	BH-PD:nppukp	Configurable I/O
AD3	GPIO_41	P3	BH-PD:nppdkp	Configurable I/O
V6	GPIO_42	P3	BH-PD:nppukp	Configurable I/O
AB1	GPIO_44	P3	BH-PD:nppukp	Configurable I/O
AA5	GPIO_45	P3	BH-PD:nppukp	Configurable I/O
V7	GPIO_47	P3	BH-PD:nppukp	Configurable I/O
W2	GPIO_49	P3	BH-PD:nppukp	Configurable I/O
V3	GPIO_50	P3	BH-PD:nppukp	Configurable I/O
V5	GPIO_52	P3	BH-PD:nppukp	Configurable I/O
G5	GPIO_55	P3	BH-PD:nppukp	Configurable I/O
H6	GPIO_56	P3	BH-PD:nppukp	Configurable I/O

Table 6-10 APQ8064 wakeup pins[a] (Continued)

Pad #	Pad name	Pad voltage	Pad type	Functional description
G6	GPIO_58	P3	BH-PD:nppukp	Configurable I/O
C6	GPIO_61	P3	BH-PD:nppukp	Configurable I/O
AC2	GPIO_63	P3	BH-PD:nppukp	Configurable I/O
AB2	GPIO_65	P3	BH-PD:nppukp	Configurable I/O
H12	GPIO_72	P3	BH-PD:nppukp	Configurable I/O
C27	GPIO_73	P3	BH-PU:nppdkp	Configurable I/O
G23	GPIO_74	P3	BH-PU:nppdkp	Configurable I/O
C26	GPIO_75	P3	BH-PU:nppdkp	Configurable I/O
F22	GPIO_76	P3	BH-PU:nppdkp	Configurable I/O
J21	GPIO_77	P3	BH-PU:nppdkp	Configurable I/O
E3	GPIO_81	P3	BH-PD:nppukp	Configurable I/O
AA21	GPIO_83	P3	BH-PD:nppukp	Configurable I/O
Y20	GPIO_84	P3	BH-PD:nppukp	Configurable I/O
H15	GPIO_88	P4	BH-PD:nppukp	Configurable I/O
B26	SDC1_DATA_3	P3	B	Secure digital controller 1 data bit 3
B25	SDC1_DATA_1	P3	B	Secure digital controller 1 data bit 1
F1	SDC3_DATA_3	P2	B	Secure digital controller 3 data bit 3 (dual-voltage)
F2	SDC3_DATA_1	P2	B	Secure digital controller 3 data bit 1 (dual-voltage)
D26	SRST_N	P3	DI	JTAG reset for debug

a. Refer to Table 6-5 for parameter and acronym definitions.

Table 6-11 APQ8064 pin descriptions – chipset interface functions [a]

Pad #	Pad name and/or function	Pad name or alt function	Pad voltage	Pad type	Functional description
GPS RF receiver IC – GNSS Rx baseband interface					
N9	GNSS_BB_IP		–	AI	GNSS receiver baseband input, in-phase plus
N8	GNSS_BB_IM		–	AI	GNSS receiver baseband input, in-phase minus
M9	GNSS_BB_QP		–	AI	GNSS receiver baseband input, quadrature plus
M8	GNSS_BB_QM		–	AI	GNSS receiver baseband input, quadrature minus
AE23	GNSS_BLANKING	GPIO_80	P3	DO B-PD:nppukp	GNSS Rx blanking control Configurable I/O
E3	SSBI_EXT_GPS	GPIO_81	P3	B BH-PD:nppukp	Single-wire serial bus interface for external GPS Configurable I/O
AC24	GPS_PPS_OUT	GPIO_6	P3	DO BH-PD:nppukp	GPS one pulse per second output Configurable I/O
AC24	GPS_PPS_IN	GPIO_6	P3	DI BH-PD:nppukp	GPS one pulse per second input Configurable I/O
PMIC interfaces					
E27	SLEEP_CLK		P3	DI	Sleep clock
E4	CXO		P3	DI	Core crystal oscillator (system clock at 19.2 MHz)

Table 6-11 APQ8064 pin descriptions – chipset interface functions [a] (Continued)

Pad #	Pad name and/or function	Pad name or alt function	Pad voltage	Pad type	Functional description
C2	CXO_EN		P3	DO	Core crystal oscillator enable
U21	RESIN_N		P3	DI	Reset input
C28	PS_HOLD	GPIO_78	P3	DO B-PD:nppukp	Power supply hold signal to PMIC Configurable I/O
E25	SSBI_PMIC1		P3	B	Single-wire serial bus interface for PMIC1
F23	SSBI_PMIC2	GPIO_79	P3	B B-PD:nppukp	Single-wire serial bus interface for PMIC2 Configurable I/O
H14	SSBI_PMIC_FCLK		P3	DO	Alternate PMIC SSBI clock when CXO is disabled
C26	Reserved	GPIO_75	P3	BH-PU:nppdkp	Configurable I/O
C27	PMIC1_SEC_INT_N	GPIO_73	P3	DI BH-PU:nppdkp	Secure apps μP interrupt request from PMIC1 Configurable I/O
G23	PMIC1_USR_INT_N	GPIO_74	P3	DI BH-PU:nppdkp	User (nonsecure) apps μP interrupt request from PMIC1 Configurable I/O
F22	PMIC2_SEC_INT_N	GPIO_76	P3	DI BH-PU:nppdkp	Secure apps μP interrupt request from PMIC2 Configurable I/O
J21	PMIC2_USR_INT_N	GPIO_77	P3	DI BH-PU:nppdkp	User (nonsecure) apps μP interrupt request from PMIC2 Configurable I/O
–	Also see Table 6-8 for UIM connectivity ports that can use the PMIC for level translation.				
–	Also see Table 6-8 for UART connectivity ports that can use the PMIC as a 3:1 UART multiplexer.				
Wireless connectivity IC – BT signals					
AC2	SSBI_BT	GPIO_63	P3	B BH-PD:nppukp	Single-wire serial bus interface for Bluetooth Configurable I/O
D3	BT_DATA_STROBE	GPIO_17	P3	B B-PD:nppukp	Bluetooth dual-function signal – serial data and strobe Configurable I/O
C3	BT_CTL	GPIO_16	P3	B-PD:nppukp	Bluetooth control signal Configurable I/O
Wireless connectivity IC – FM radio signals					
H9	SSBI_FM	GPIO_14	P3	B B-PD:nppukp	Single-wire serial bus interface for FM radio Configurable I/O
F6	FM_SDI	GPIO_15	P3	B BH-PD:nppukp	FM radio serial data interface Configurable I/O
Wireless connectivity IC – shared BT/FM radio signals					
AC4	WCN_XO		P3	DI	Shared XO for the wireless connectivity subsystem
Audio codec IC interfaces					
–	See Table 6-8 for SLIMbus bidirectional mutliplexed audio (AUD_SB1).				
–	Also see Table 6-8 for I^2C connectivity ports that can used as the status and control interface.				
Mobile broadcast platform interfaces					
–	See Table 6-8 for SD connectivity ports that can used as the host controller interface.				
–	Also see Table 6-8 for SPI connectivity ports (via GSBI) that can used as the host controller interface.				
–	Also see Table 6-8 for TSIF connectivity ports that can used for MPEG packet transfers in ISDB-T applications.				

a. Refer to Table 6-5 for parameter and acronym definitions.

NOTE GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the table above), designers must identify all their application's requirements and map each GPIO to its function – carefully avoiding conflicts in GPIO assignments. Refer to Chapter 11 – GPIO for a list of all supported functions for each GPIO.

6.5.4 GPIO

For GPIO and GSBI information, see Chapter 11 – GPIO for more information.

6.5.5 Other pin tables

6.5.5.1 Do not connect

Table 6-12 APQ8064 pin descriptions – no connection and do not connect pins

Pad #	Pad name	Functional description
A1, A2, A27, A28, B1, B2, B27, B28, C1, C8, C10, C12, C14, C15, C17, C19, C21, D2, D4, D8, D10, D12, D14, D15, D17, D19, D21, E2, E10, E14, E15, E19, F10, F12, F17, F19, G10, G12, G17, G19, H3, H4, H25, H26, K3, K4, K5, K6, K7, K23, K24, K25, K26, M3, M4, M6, M7, M25, M26, P3, P4, P5, P24, P25, P26, R3, R4, R5, R24, R25, R26, U3, U4, U6, U7, U25, U26, W3, W4, W5, W6, W7, W23, W24, W25, W26, AA3, AA4, AA7, AA25, AA26, AB8, AB10, AB12, AB17, AB19, AB21, AC10, AC12, AC17, AC19, AC21, AD10, AD14, AD15, AD19, AE8, AE10, AE12, AE14, AE15, AE17, AE19, AF8, AF10, AF12, AF14, AF15, AF17, AF19, AF21, AG1, AG2, AG27, AG28, AH1, AH2, AH27, AH28	DNC	Do not connect; connected internally, do not connect externally

Table 6-13 APQ8064 pin descriptions – power supply pins

Pad #	Pad name	Functional description
AB18	VDD_A2	Power for analog circuits – high voltage
F3, H21, J4, J16, J17, K10, K11, L11, M5, M12, M13, M17, N13, N20, P10, P11, P17, R6, R11, T12, T13, U13, V17, W17	VDD_CORE	Power for digital core circuits
R15, R16, T15, T16	VDD_KR0	Power for Krait application microprocessor 0
U23	VDD_KR0_SNS	Sense node for Krait application microprocessor 0 supply voltage
R18, R19, T18, T19	VDD_KR1	Power for Krait application microprocessor 1
U22	VDD_KR1_SNS	Sense node for Krait application microprocessor 1 supply voltage
L15, L16, M15, M16	VDD_KR2	Power for Krait application microprocessor 2
M23	VDD_KR2_SNS	Sense node for Krait application microprocessor 2 supply voltage
L18, L19, M18, M19	VDD_KR3	Power for Krait application microprocessor 3
M22	VDD_KR3_SNS	Sense node for Krait application microprocessor 3 supply voltage
J9, J12, J15, J18, J19, L10, M21, N12, N16, N18, R10, U12, U18, V16, V19, W9, W11	VDD_MEM	Power for on-chip memory
G8, G21, H7, H11, H19, H22, M20, V8, V18, V21, Y7, AA22	VDD_P1	Power for pad group 1 – EBI0 and EBI1 pads
F5	VDD_P2	Power for pad group 2 – SDC3 pads
D5, F26, H13, H20, J6, R20, U5, W19, Y5, AC20, AE25	VDD_P3	Power for pad group 3 – most I/O pads
H16	VDD_P4	Power for pad group 4 – HSIC pads
J20, K9	VREF_DDR_C1	VREF for channel 1 of PCDDR memory
N21, V9, W20	VREF_DDR_C0	VREF for channel 0 of PCDDR memory

Table 6-13 APQ8064 pin descriptions – power supply pins (Continued)

Pad #	Pad name	Functional description
AA15, Y16	VDD_HDMI	Power for HDMI circuits
Y8, AA9, AA10, AC5	VDD_MIPI	Power for MIPI circuits (CSI and DSI)
Y13, AD11	VDD_LVDS	Power for LVDS circuits
V14, N14, J14	VDD_PLL1	Power for PLL circuits – low voltage
K13, K14, K20, N15, U10, U14, U20	VDD_PLL2	Power for PLL circuits – high voltage
W13	VDD_PXO	Power for platform crystal oscillator circuits
J8	VDD_QFUSE_PRG	Power for programming Q-fuses; otherwise connect to ground
U11, V10, V11	VDD_QDSP6	Power for QDSP6 – application processor
T1	VDD_USBPHY1_1P8	Power for USB PHY interface 1 – low voltage
P1	VDD_USBPHY1_3P3	Power for USB PHY interface 1 – high voltage
J3	VDD_USBPHY3_1P8	Power for USB PHY interface 3 – low voltage
J1	VDD_USBPHY3_3P3	Power for USB PHY interface 3 – high voltage
N6	VDD_USBPHY4_1P8	Power for USB PHY interface 4 – low voltage
L1	VDD_USBPHY4_3P3	Power for USB PHY interface 4 – high voltage
N7	VDDA_GPS	Power for GPS circuits
AA18, AD18	VDDA_PCIE	Power for PCIe interface
AA17, AC16	VDD_SATA	Power for Serial ATA circuits
G4	VREF_SDC	Reference voltage for secure digital controller circuits

Table 6-14 APQ8064 pin descriptions – ground pins

Pad #	Pad name	Functional description
C5, C9, C13, C16, C20, C23, E11, E18, E26, F4, G7, G9, G13, G16, G20, G22, H1, J2, J5, J7, J10, J13, J22, J26, K8, K12, K15, K16, K17, K18, K19, K22, L2, L3, L6, L8, L9, L12, L13, L14, L17, L20, L24, M10, M11, M14, N2, N10, N11, N17, N19, N22, N26, P2, P6, P7, P8, P12, P13, P14, P15, P16, P18, P19, R7, R12, R13, R14, R17, T2, T6, T10, T11, T14, T17, T20, T22, T26, U9, U15, U16, U17, U19, V2, V12, V13, V15, V20, V24, W8, W10, W12, W16, W18, W22, Y4, Y14, Y15, Y17, Y18, Y19, Y22, Y26, AA8, AA16, AA19, AB6, AB11, AB16, AB20, AB22, AB23, AC6, AC26, AD4, AD6, AD20, AD28, AE1, AE2, AE3, AE18, AE20, AE24, AE27, AE28, AF3, AF4, AF18, AF20, AF28, AG18, AG22, AH18, AH22, AH23, AH24, AH25, AH26	GND	Ground

6.6 Device reset

Four types of reset; available resets depend on the boot mode (Boot Overview):

- Cold boot
  - Poweron reset via PMIC (IC-level Interfaces)
- Warm boot
  - Watchdog-expired reset
  - Software system reset via register write

6.7 Default device configurations

This information will be included in future revisions of this document.

6.8 Power domain

See Chapter 8 – Device Operating Conditions for more information.

7 System Interconnect (FABRIC)

The APQ8064 device uses a tiered interconnect:

- Provides a low latency path from the Krait processor subsystem (KPSS) to the external EBI1 memory
- System FABRIC is the main system bus with all the masters and slaves connected to it directly or through other interconnects
  - The system FABRIC can be run at a maximum clock frequency of 133 MHz at 0.945V and 177 MHz at 1.055V
  - 15 x 15 System FABRIC. Bus ID = 1; 133 MHz Operation; 64-bit internal bus

The System FABRIC interconnects the following subtending FABRIC configurations:

- 3 x 4 Daytona FABRIC. Bus ID = 0; 64 MHz operation; 32-bit internal bus
- 13 x 3 Multimedia Subsystem. Bus ID = 3; 166 MHz Operation; 128-bit internal bus
- 6 x 5 Apps FABRIC. Bus ID = 2; 400 MHz Operation; 64-bit internal bus

8 Device Operating Conditions

Operating conditions include parameters that are under the control of the user: power-supply voltage and ambient temperature (Table 8-1). The APQ8064 meets all performance specifications listed in this document when used within the recommended operating conditions, unless otherwise noted in those sections (provided the absolute maximum ratings have never been exceeded).

Table 8-1 Recommended operating conditions [a]

Parameter		Min	Typ [d]	Max	Unit
Power-supply voltages					
V_{DD_PXO}	Power supply for platform oscillator (27 MHz)	1.03	1.10	1.17	V
V_{DD_A2}	Analog 2 circuits – high voltage	1.674	1.80	1.98	V
V_{DD_MIPI}	Power for MIPI circuits (CSI and DSI)	1.11	1.17	1.23	V
V_{DD_HDMI}	Power for HDMI circuits	1.70	1.80	1.95	V
V_{DD_PLL1}	Power for low-voltage PLL circuits	0.975	1.05	1.225	V
V_{DD_PLL2}	Power for high-voltage PLL circuits	1.70	1.80	1.95	V
Power-supply voltages – memory					
V_{DD_MEM} [b]	APQ internal system memory	0.975	1.05	1.125	V
Power-supply voltages – processors					
V_{DD_CORE}	Digital core				
High		1.075	1.15	1.225	V
Nominal		0.975	1.05	1.125	V
Low		0.9	0.95	1.00	V
V_{DD_QDSP6}	QDSP6 application processor circuits				
PVS = 000		0.925	0.975	1.025	V
PVS = 001		0.90	0.90	0.95	V
PVS = 010		0.85	0.85	0.90	V

Table 8-1 Recommended operating conditions [a] (Continued)

Parameter		Min	Typ [d]	Max	Unit
V_{DD_KR0}, V_{DD_KR1}, V_{DD_KR2}, V_{DD_KR3}	Krait application microprocessor 0, 1, 2, and 3 operating at 1512 MHz [c]				
PVS = 000		1.20	1.25	1.30	V
PVS = 001		1.15	1.20	1.25	V
PVS = 010		1.10	1.15	1.20	V
Power-supply voltages – pads					
V_{DD_P1}	Pad group 1 – EBI0 and EBI1	1.14	1.2	1.3	V
V_{DD_P2}	Pad group 2 – dual voltage SDC3 (1.8 V or 2.95 V)	2.75	2.95	3.00	V
	2.95 V	1.70	1.80	1.95	V
	1.80 V				
V_{DD_P3}	Pad group 3 – most pads and peripheral I/Os	1.70	1.80	1.95	V
V_{DD_P4}	Pad group 4 – HSIC I/O	–	–	–	
Used as GPIO		1.70	1.80	1.95	V
Used as HSIC		1.15	1.20	1.25	V
$V_{DD\_QFUSE\_PRG}$	Qfuse programming voltage	1.65	1.80	1.95	V
$V_{DD\_USBPHYX\_1P8}$	USB PHY pad group (1.8 V)	1.73	1.80	1.87	V
$V_{DD\_USBPHYX\_3P3}$	USB PHY pad group (3.3 V)	2.97	3.3 [e]	3.63	V
Thermal condition					
T_C	Operating temperature (case)	-30	+25	+90	°C

a. The maximum and minimum data are preliminary and are subject to change based on characterization results.

b. VDD_MEM is required to be greater than VDD_CORE, VDD_QDSP6, VDD_KR0, VDD_KR1, VDD_KR2, and VDD_KR3. The min/max/typ voltages for all processor rails depend on the processor speed configuration.

c. **IMPORTANT:** The The following PCB impedances are believed to be required to meet the min and max voltage specifications. If these PCB impedances cannot be achieved, contact Computing, Inc immediately.

Power domain	DC–300 kHz	300 kHz–25 MHz
V_{DD_CORE}	≤ 10 mΩ	25 mΩ
V_{DD_KR0}	≤15 mΩ	54 mΩ
V_{DD_KR1}		
V_{DD_KR2}		
V_{DD_KR3}		
$V_{DD\_QDSP6\_APP}$	≤ 10 mΩ	65 mΩ
V_{DD_MEM}	≤ 10 mΩ	30 mΩ

Power domain	DC – 10 Hz	10 Hz – 25 MHz
V_{DD_CORE}	≤ 10 mΩ	25 mΩ
V_{DD_KR0} V_{DD_KR1}	≤ 10 mΩ	25 mΩ
$V_{DD\_QDSP6\_APP}$ $V_{DD\_QDSP6\_MFW}$ $V_{DD\_QDSP6\_MSW}$	≤ 10 mΩ	65 mΩ 75 mΩ 65 mΩ
V_{DD_MEM}	≤ 10 mΩ	30 mΩ

d. Typical voltages represent the recommended output settings of the PMICs.

e. The companion PMIC currently sets the USB PHY 3.3 V rail to 3.075 V by default, due to power considerations. Customers need to ensure that, at a minimum, 2.97 V is observed on the VDD_USBPHY_3P3 pin so that it is within the USB PHY design specifications.

9 Peripheral Information and Electrical Specifications

9.1 Recommended clock and control signal transition behavior

Some internal functions require external interfaces to enable their operation. These include clock generation, modes and resets, and JTAG functions – as specified in the following subsections.

9.1.1 Clocks

Clocks that are specific to particular functions are addressed in the corresponding sections of this document. Others are specified here.

9.1.1.1 19.2 MHz core XO input

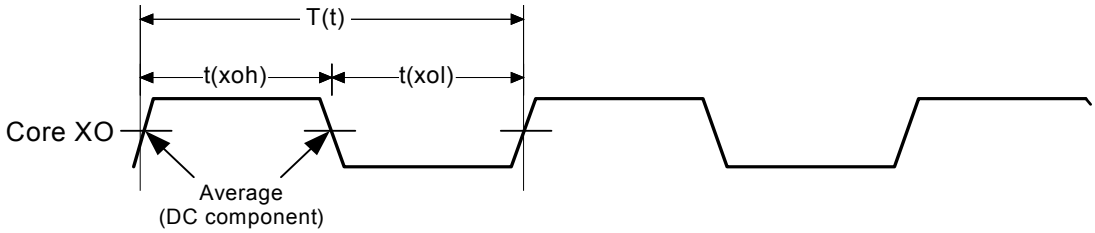

Figure 9-1 Core XO timing parameters

Table 9-1 Core XO timing parameters [a]

Parameter		Comments	Min	Typ	Max	Unit
t(xoh)	Core XO logic high		22.6	–	29.5	ns
t(xol)	Core XO logic low		22.6	–	29.5	ns
T(t)	Core XO clock period		–	52.083	–	ns
1/T(t)	Frequency	19.2 MHz must be used.	–	19.2	–	MHz

a. For more information, refer to LM80-P0598-8, *GPS Quality, 19.2 MHz 2520 Package Size, Crystal and TH+Xtal Mini-Specification* document.

9.1.1.2 Sleep clock

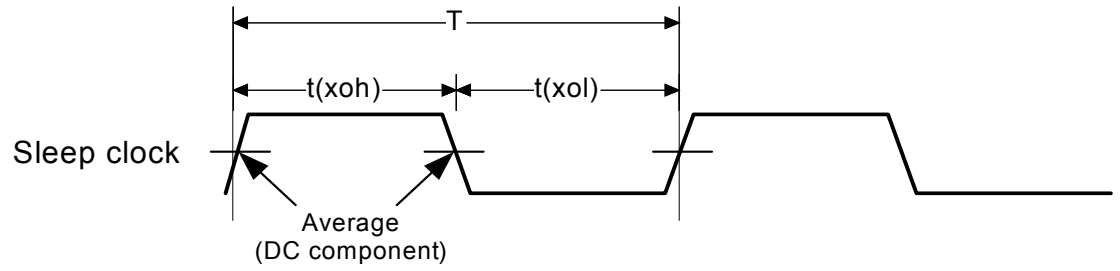

Figure 9-2 Sleep-clock timing parameters

Table 9-2 Sleep-clock timing parameters

Parameter		Comments	Min	Typ	Max	Unit
t(xoh)	Sleep-clock logic high		4.58	–	25.94	µs
t(xol)	Sleep-clock logic low		4.58	–	25.94	µs
T(t)	Sleep-clock period		–	30.518	–	µs
1/T(t)	Frequency		–	32.768	–	kHz

9.1.1.3 PXO (27 MHz) crystal oscillator

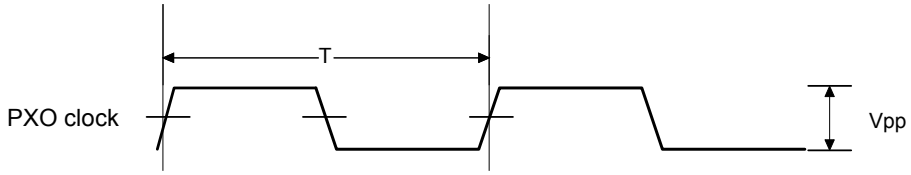

Figure 9-3 PXO (27 MHz) crystal oscillator timing parameters

Table 9-3 PXO (27 MHz) crystal oscillator parameters

Parameter	Min	Typ	Max	Unit
Frequency	–	27	–	MHz
Frequency tolerance	-30	–	30	ppm
Series resistance (ESR)	–	–	60	Ω
Load capacitance	11	15	17	pF
Shunt capacitance	–	–	5	pF

9.1.2 PMIC

The PMM8920 device is a module that integrates two power management die (PM8921 and PM8821) into a single package.

9.1.2.1 PM8921 die

The PMIC includes several clock circuits whose outputs are used for general housekeeping functions, and elsewhere within the system. These circuits include a 19.2 MHz XO with multiple controllers and buffers, an MP3 clock output, 32.768 kHz crystal support, an RC oscillator, sleep clock outputs, and internal SMPL and SMPS clocks. Performance specifications for these functions are presented in the following subsections.

9.1.2.1.1 19.2 MHz XO circuits

An external crystal is supplemented by on-chip circuits to generate the desired 19.2 MHz reference signal. Using an external thermistor network, the on-chip ADC, and advanced temperature compensation software, the PMIC eliminates the large and expensive VCTCXO module required by previous generation chipsets. The XO circuits initialize and maintain valid pulse waveforms and measure time intervals for higher-level device functions. Multiple controllers manage the XO warmup and signal buffering, and generate the desired clock outputs (all derived from one source):

- XO_OUT_A0
- XO_OUT_A1
- XO_OUT_A2
- XO_OUT_D0
- XO_OUT_D1

Since the different controllers and outputs are independent of each other, non-phone circuits can operate even while the phone's baseband circuits are asleep and its RF circuits are powered down.

The PM8921 IC has built-in load capacitors on XTAL_19M_IN and XTAL_19M_OUT. A crystal that specifies 7 pF load caps is recommended because no external load capacitors will be required. This reduces the noise picked up from the GND plane.

The XTAL_19M_IN and XTAL_19M_OUT pins are incapable of driving a load – the oscillator will be significantly disrupted if either pin is externally loaded.

As discussed in Section 9.1.2.1.5, an RC oscillator is used to drive some clock circuits until the XO source is established.

Table 9-4 Specifications for XO_OUT_D0 and XO_OUT_D1

Parameter	Comments	Min	Typ	Max	Unit
Frequency	Set by external crystal	–	19.2	–	MHz
Output duty cycle[a]		46	50	60	%
USB 2.0 jitter	Specified values are peak-to-peak period jitter				
0.5 MHz – 2 MHz[b]		–	–	50	ps
> 2 MHz		–	–	100	ps
Startup time[c]		–	–	6	ms
Current consumption		0.94	0.98	1.0	mA
Supply voltage		1.782	1.80	1.818	V
Buffer output impedance[d]					
at 1x drive strength		54	80	122	Ω / mA
at 2x drive strength		30	42	64	Ω / mA
at 3x drive strength		21	30	44	Ω / mA
at 4x drive strength		17	22	35	Ω / mA

a. Duty cycle is defined as the first pulse duty cycle that meets the overall duty cycle specification

b. USB period jitter can be calculated by 14 · Jit_{ter}rms based on the ^{10}-12 BER requirement

c. When the warmup time enhancement feature is enabled, this can be reduced to 3.5 ms (to be finalized after analysis of more characterization data

d. Output impedance at each drive strength varies 30% over corners. Current drive capabilities included to meet VOH = 0.65 · VDD and VOL = 0.35 · VD

9.1.2.1.2 Typical 19.2 MHz XO crystal requirements

Table 9-5 Typical 19.2 MHz crystal specifications (2520 size)

Parameter	Comments	Min	Typ	Max	Units
Operating frequency		–	19.2	–	MHz
Mode of vibration		–	AT-cut fundamental	–	–
Initial frequency tolerance		–	–	±10	PPM
Tolerance over temperature		–	–	±12	PPM
Aging		–	–	±1	PPM/year
Frequency drift after reflow	After two reflows	–	–	±2	PPM
Operating temperature		-30	–	+85	^{0}C
Storage temperature		-40	–	+85	^{0}C
Equivalent series resistance	New for 2520 crystals		–	80	W
Quality factor (Q)	Minimum Q value calculated from ESR and L is smaller than this specification	75,000	–	–	–
Spurious mode series resistance	±1 MHz	1100	–	–	W

Table 9-5 Typical 19.2 MHz crystal specifications (2520 size) (Continued)

Parameter	Comments	Min	Typ	Max	Units
Motional capacitance	New for 2520 crystals	1.80	–	3.10	fF
Shunt capacitance		0.3	–	1.3	pF
Load capacitance	Load capacitance is measured according to IEC standard #60444-7	–	7	–	pF
Third-order curve fitting parameter	Curve fitting parameter is obtained from the crystal curve-fitting algorithm	8.5	10	11.5	e-5
Drive level		10	–	100	µW
Insulation resistance		500	–	–	MΩ
Package size		–	2.5 × 2.0	–	mm

Table 9-6 Specifications for XO_OUT_A0, XO_OUT_A1, and XO_OUT_A2

Parameter	Comments	Min	Typ	Max	Unit
Frequency	Set by external crystal	–	19.2	–	MHz
Duty cycle		40	50.0	60.0	%
Startup time[a]		–	6	–	ms
Current consumption[b]					
HPM		0.89	1.14	1.38	mA
NPM		1.11	1.23	1.52	mA
LPM		1.23	1.39	1.74	mA
Output voltage swing		1.2	–	1.8	V
Buffer output impedance[c]					
at 1x drive strength		54	80	122	Ω / mA
at 2x drive strength		30	42	64	Ω / mA
at 3x drive strength		21	30	44	Ω / mA
at 4x drive strength		17	22	35	Ω / mA
Phase noise in LPM					
at 10 Hz		–	–	-86	dBc/Hz
at 100 Hz		–	–	-110	dBc/Hz
at 1 kHz		–	–	-124	dBc/Hz
at 10 kHz		–	–	-134	dBc/Hz
at 100 kHz		–	–	-140	dBc/Hz
at 1 MHz		–	–	-137	dBc/Hz

Table 9-6 Specifications for XO_OUT_A0, XO_OUT_A1, and XO_OUT_A2

Parameter	Comments	Min	Typ	Max	Unit
Phase noise in NPM					
at 10 Hz		–	–	-86	dBc/Hz
at 100 Hz		–	–	-116	dBc/Hz
at 1 kHz		–	–	-134	dBc/Hz
at 10 kHz		–	–	-144	dBc/Hz
at 100 kHz		–	–	-144	dBc/Hz
at 1 MHz		–	–	-144	dBc/Hz
Phase noise in HPM					
at 10 Hz		–	–	-86	dBc/Hz
at 100 Hz		–	–	-116	dBc/Hz
at 1 kHz		–	–	-134	dBc/Hz
at 10 kHz		–	–	-144	dBc/Hz
at 100 kHz		–	–	-148	dBc/Hz
at 1 MHz		–	–	-150	dBc/Hz

a. The startup time corresponds to the time taken by the buffer to output the first valid pulse that meets the overall duty-cycle specification. When the warmup time enhancement feature is enabled, this can be reduced to 3.5 m

b. Includes 15 pF load cap, output swing = 1.8

c. Output impedance at each drive strength varies 30% over corners. Current drive capabilities included to meet VOH = 0.65 · VDD and VOL = 0.35 · VD

9.1.2.1.3 MP3 clock

One GPIO can be configured as a 2.4 MHz clock output to support MP3 in a low-power mode. This clock is a divided down version of the 19.2 MHz XO signal, so its most critical performance features are defined within the XO tables (Section 9.1.2.1.1). Output characteristics (voltage levels, drive strength, etc.) are defined in Section 9.5.3.

9.1.2.1.4 32 kHz oscillator

The following are three options for implementing the 32 kHz oscillator:

- Using the XO signal (19.2 MHz)
- An external 32.768 kHz crystal oscillator
- An external oscillator module

Whichever method is used, this oscillator signal is the primary sleep clock source. In all cases, neither the XTAL_32K_IN nor the XTAL_32K_OUT pins are capable of driving a load – the oscillator will be significantly disrupted if either pin is loaded.

The PMIC includes a circuit that continually monitors this oscillation. If the circuit is enabled but stops oscillating, the device automatically switches to the internal RC oscillator and generates an interrupt.

Performance specifications pertaining to the 32 kHz oscillator are listed in Table 9-7.

Table 9-7 Typical 32 kHz crystal specification

Parameter	Comments	Min	Typ	Max	Unit
Nominal oscillation frequency	F	–	32.768	–	kHz
Load capacitance	CL	7	–	12.5	pF
Frequency tolerance	ΔF/F	-100		100	ppm
Drive level	P	–	0.1	1	µW
Aging first year	ΔF/F	-3	–	3	ppm
Series resistance	Rs	–	50	80	kΩ
Motional capacitance	C1	–	2.1	–	fF
Static capacitance	C0	–	0.9	–	pF

9.1.2.1.5 RC oscillator

As mentioned in previous sections, the PMIC includes an on-chip RC oscillator that is used during startup and as a backup to the 32 kHz oscillator. Pertinent performance specifications are listed in Table 9-8.

Table 9-8 RC oscillator performance specifications

Parameter	Comments	Min	Typ	Max	Units
Oscillation frequency		14	19.2	24	MHz
Duty cycle		30	50	70	%
Divider in SLEEP_CLK path		–	586	–	–

9.1.2.1.6 Sleep clock

The sleep clock is generated one of three ways:

- Using the 19.2 MHz XO circuit and dividing its output by 586 to create a 32.7645 kHz signal – this method supports all normal operating modes.
- Using the 32.768 kHz crystal and supporting PMIC circuits – this method supports all normal operating modes.
- Using the on-chip 19.2 MHz RC oscillator and divide-by-586 to create a coarse 32 kHz signal – this method is only used during startup and if the 32.768 kHz XTAL source fails.

The PMIC sleep clock output is routed to the APQ device circuits using the SLEEP_CLK0 pin. It is also available for other applications via GPIO_43 and GPIO_44 when configured properly (as SLEEP_CLK1 and SLEEP_CLK2, respectively).

These clock outputs are derived from other sources specified earlier:

- 19.2 MHz XO circuits (Section 9.1.2.1.1)
- 32.768 kHz XTAL oscillator (Section 9.1.2.1.4)
- 19.2 MHz RC oscillator (Section 9.1.2.1.5)

Output characteristics (voltage levels, drive strength, etc.) are defined in Section 9.5.3.

9.1.2.2 PM8821 die

Most housekeeping functions are provided by the PM8921 IC, so the PM8821 IC needs only supplement with the 19.2 MHz clock.

9.1.2.2.1 19.2 MHz clock

The PM8921 IC supplements the PM8821 IC with clock circuits that can accept the 19.2 MHz XO signal from PM8921 or can generate its own using an on-chip RC oscillator. Pertinent performance specifications are presented in the following subsections.

9.1.2.2.2 XO signal from PM8921 IC

One of the PM8921 digital XO signals (XO_OUT_D1) can be routed to the PM8821 SSBI_CLK pin, rather than using the on-chip oscillator circuit. The two PMICs are guaranteed to work together using this configuration, so additional performance specifications are not required.

9.1.2.2.3 RC oscillator

The on-chip RC oscillator is the default clock option for the PM8821 SMPS modules. Pertinent performance specifications are listed in Table 9-9.

Table 9-9 RC oscillator performance specifications

Parameter	Comments	Min	Typ	Max	Unit
Oscillation frequency		14	19.2	24	MHz
Duty cycle		30	50	70	%

9.1.2.2.4 Overtemperature protection (smart thermal control)

The PMIC includes overtemperature protection in stages, depending on the level of urgency as the die temperature rises:

- Stage 0 – normal operating conditions (less than 105°C).
- Stage 1 – 105°C to 110°C; an interrupt is sent to the APQ device without shutting down any PMIC circuits.
- Stage 2 – 110°C to 130°C; an interrupt is sent to the APQ device and high-current circuitry may be shut down.
- Stage 3 – greater than 150°C; an interrupt is sent to the APQ device and the PMIC is completely shut down.

Temperature hysteresis is incorporated so that the die temperature must cool significantly before the device can be powered on again. If any start signals are present while at Stage 3, they are ignored until Stage 0 is reached. When the device cools enough to reach Stage 0 and a start signal is present, the PMIC will power up immediately.

9.2 Power supplies

Power supplies are listed in the table Table 9-10.

Table 9-10 Power supplies

Domain Description	Parameter	Min	Typ	Max	Unit
Digital core (Vddcx) VDD_DIG regulator	Voltage	0.945 Nom. 0.85 SVS	1.050	1.260	V
	Idle current	1170	3780	6630	mA
Memory (Vddmx) VDD_MEM regulator	Voltage	0.945	1.050	1.260	V
VDD_DAC	Voltage	1.75	1.8	1.9	V
	Current	0	N/A	16	mA
VDD_ADC	Voltage	1.75	1.8	1.9	V
	Power	0	N/A	23	mW
VDD_GNSS_ADC	Voltage	1.225	1.3	1.35	V
	Power	0	N/A	1.7	mW
VDD_FWQ6	Voltage	0.945 Nom. 0.85 SVS	1.050	1.260	V
VDD_SWQ6	Voltage	0.945 Nom. 0.85 SVS	1.050	1.260	V

NOTE Peak current is not specified as it is heavily software and scenario dependent.

9.3 Power supply sequencing

9.3.1 PMM8920 device

The PMM8920 includes poweron circuits that provide the proper power sequencing for the entire APQ8064 chipset. The supplies are turned on as groups of regulators that are selected by the hardware configuration of some PMIC pins.

For more information, refer to LM80-P0598-4, *PMM8920 Power Management Module Device Specification* document.

A high-level summary of the APQ8064's required early powerup sequence is as follows:

1. V_{DD_MEM} / V_{DD_PLL1}
2. V_{DD_CORE}
3. $V_{DD\_P3(GPIO)}$
4. $V_{DD\_P1(EBI)}$
5. VREF_DDR_C1 / VREF_DDR_C2
6. V_{DD_PXO}

7. $V_{DD\_USBPHYX\_1P8}$ (HS USB 1.8 V)
8. V_{DD_P2} (SDC 2.95 V)
9. T-FLASH (SD VDD)
10. $V_{DD\_USBPHYX\_3P3}$ (HS USB 3.3 V)
11. eMMC VCC

Comments regarding this sequence:

- The core voltage (V_{DD_CORE}) needs to power up before the pad circuits (V_{DD_PX}) so that internal circuits can take control of the I/Os and pads.
  - If pad voltages power up first, the output drivers might be stuck in unknown states, and might cause large leakage currents until V_{DD_CORE} powers on.
- The pad voltages need to precede the analog voltages (V_{DD_AX}), since the SSBIs are initialized to their default states before V_{DD_AX} powers up (analog circuits are controlled by SSBI).
- V_{DD_QDSP6}, V_{DD_KR0}, V_{DD_KR1}, V_{DD_KR2} and V_{DD_KR3} (QDSP and Krait core circuits) can be powered up by software after the APQ has completed the boot process.
- Other non-critical supplies are included within the poweron sequence. Any other desired supplies can be powered on by software after the sequence is completed.
- Each domain needs to reach its 90% value before the next domain starts ramping up. For example, when V_{DD_CORE} reaches 90% of its value, the V_{DD_P3} supply can start ramping up.

NOTE $V_{DD\_QFUSE\_PRG}$ must be powered down before any of the pad power supplies are powered down.

9.3.2 PM8821 device

PM8821 power sequences are initiated when the PM8921 device drives PON_RESET_N high.

The PM8821 PON_RESET_N signal is not used since the PM8921 device will assert PON_RESET_N high to both the PM8821 device and the APQ simultaneously. The PM8821 does not have any default-on regulators except for VDD_DIG, which is only used internally for PM8821. Therefore, there is no defined poweron sequence for the PM8821 device.

9.4 Reset

There are four types of reset; available resets depend upon the boot mode (see Section 6.2):

- Cold boot
  - Power-on reset via the PMIC
- Warm boot
  - Power restore reset

- Watchdog-expired reset
- Software system reset via register write

9.5 Chipset electrical specification

9.5.1 Absolute maximum ratings

Operating the APQ8064 under conditions beyond its absolute maximum ratings (listed in Table 9-11) may damage the device. Absolute maximum ratings are limiting values to be considered individually when all other parameters are within their specified operating ranges. Functional operation and specification compliance under any absolute maximum condition, or after exposure to any of these conditions, is not guaranteed or implied. Exposure may affect device reliability.

Table 9-11 Absolute maximum ratings

Parameter		Min	Max	Unit
Power supply voltages				
V_{DD_AX}	Analog circuits	–	V_{DD_AX} * 1.5	V
V_{DD_CORE}	Digital core circuits	–	1.65	V
V_{DD_MEM}	APQ internal memory	–	1.8	V
V_{DD_PX}	Digital pad circuits	–	V_{DD_PX} * 1.5	V
V_{DD_QDSP6}	QDSP6 circuits	–	1.65	V
V_{DD_KRX}	Krait core circuits	–	1.5	V
$V_{DD\_USBPHY\_1P8}$	USB PHY low voltage circuit	–	1.98	V
$V_{DD\_USBPHY\_3P3}$	USB PHY high voltage circuit	–	4.95	V
$V_{DD\_QFUSE\_PRG}$	Qfuse programming voltage	–	1.8	V
Signal pins				
V_{IN}	Voltage on any non-power input or output supply pin	–	V_{DD} + 0.5	V
I_{IN}	Latch-up current	-100	100	mA

9.5.2 Power sequencing

The PM8921 includes poweron circuits that provide the proper power sequencing for the entire APQ8064 chipset. The supplies are turned on as groups of regulators that are selected by the hardware configuration of some PMIC pins.

A high-level summary of the APQ8064 chipset's required early powerup sequence is:

1. V_{DD_MEM/VDD_PLL1}
2. V_{DD_CORE}
3. $V_{DD\_P3(GPIO)/VDD\_DDR\_C1}$

4. $V_{DD\_P1(EBI)/VDD\_DDR\_C2}$
5. V_{DD_PXO}
6. $V_{DDA\_USB\_HS\_1P8}$ (HS USB 1.8 V)
7. V_{DD_P2} (SDC 2.95 V)
8. T-FLASH (SD VDD)
9. $V_{DDA\_USB\_HS\_3P3}$ (HS USB 3.3 V)
10. eMMC VCC

Comments regarding this sequence:

- The core voltage (V_{DD_C1}) needs to power up before the pad circuits (V_{DD_PX}) so that internal circuits can take control of the I/Os and pads.
  - If pad voltages power up first, the output drivers might be stuck in unknown states, and might cause large leakage currents until VDD_C1 powers on.
- The pad voltages need to precede the analog voltages (V_{DD_AX}), since the SSBIs are initialized to their default states before V_{DD_AX} powers up (analog circuits are controlled by SSBI).
- $V_{DD\_QDSP6\_XXX}$, V_{DD_KR0}, and V_{DD_KR1}(QDSP and Krait core circuits) can be powered up by software after the APQ has completed the boot process.
- Other non-critical supplies are included within the poweron sequence. Any other desired supplies can be powered on by software after the sequence is completed.
- Each domain needs to reach its 90% value before the next domain starts ramping up. For example, when V_{DD_CORE} reaches 90% of its value, the V_{DD_P3} supply can start ramping up.

NOTE $V_{DD\_QFUSE\_PRG}$ must be powered down before any of the pad power supplies are powered down.

The VDD_QFUSE_PRG pin should be connected to a 1.8 V power supply ***only*** when blowing fuses. When not blowing fuses, this pin must be grounded and must never be left floating.

9.5.3 Digital logic characteristics

Specifications for the digital I/Os depend upon the pad voltage being used. Logic specifications are listed in Table 9-12, Table 9-13, and Table 9-14 for V_{DD_PX} = 1.8 V (P3 for most pad circuits), V_{DD_PX} = 1.2 V (P1 for EBI1), and V_{DD_PX} = 2.85 V (SD card interface), respectively.

Table 9-12 Digital I/O characteristics for V_{DD_PX} = 1.8 V nominal

Parameter		Comments	Min	Max	Unit
V_{IH}	High-level input voltage	CMOS/Schmitt	0.65 * V_{DD_PX}	V_{DD_PX} + 0.3	V
V_{IL}	Low-level input voltage	CMOS/Schmitt	-0.3	0.35 * V_{DD_PX}	V
V_{SHYS}	Schmitt hysteresis voltage		100	–	mV
I_{IH}	Input high leakage current [a, b]	No pulldown	–	1	µA

Table 9-12 Digital I/O characteristics for V_{DD_PX} = 1.8 V nominal (Continued)

Parameter		Comments	Min	Max	Unit
I_{IL}	Input low leakage current [b, c]	No pullup	-1	–	µA
I_{IHPD}	Input high leakage current [a, c]	With pulldown	5	30	µA
I_{ILPU}	Input low leakage current [b, c]	With pullup	-30	-5	µA
V_{OH}	High-level output voltage [d]	CMOS, at pin-rated drive strength	V_{DD_PX} - 0.45	V_{DD_PX}	V
V_{OL}	Low-level output voltage [d]	CMOS, at pin-rated drive strength	0	0.45	V
I_{OZH}	Tri-state leakage current [a]	Logic high output, no pulldown	–	1	µA
I_{OZL}	Tri-state leakage current[b]	Logic low output, no pullup	-1	–	µA
I_{OZHPD}	Tri-state leakage current [a, c]	Logic high output with pulldown	5	30	µA
I_{OZLPU}	Tri-state leakage current [b, c]	Logic low output with pullup	-30	-5	µA
I_{OZHKP}	Tri-state leakage current [a, c]	Logic high output with keeper	-15	-3	µA
I_{OZLKP}	Tri-state leakage current [b, c]	Logic low output with keeper	3	15	µA
I_{ISL}	Sleep crystal input leakage		-0.15	0.15	µA
I_{IHVKP}	High-V tolerant input leakage	With keeper	-1	–	µA
C_{IN}	Input capacitance [e]		–	5	pF

a. Pin voltage = V_{DD_PX} max. For keeper pins, pin voltage = V_{DD_PX} max - 0.45 V.
b. Pin voltage = GND and supply = V_{DD_PX} max. For keeper pins, pin voltage = 0.45 V and supply = V_{DD_PX} max.
c. Refer to Table 11-1 for pullup, pulldown, and keeper details.
d. Refer to Table 11-1 for each output pin's drive strength (I_{OH} and I_{OL}); the drive strengths of many output pins are programmable and depend on the associated supply voltage.
e. Input capacitance is guaranteed by design, but is not 100% tested.

Table 9-13 Digital I/O characteristics for V_{DD_PX} = 1.2 V nominal

Parameter		Comments	Min	Max	Unit
V_{IH}	High-level input voltage[a]	CMOS	V_{ref} + 0.13 V	–	V
V_{IL}	Low-level input voltage[a]	CMOS	–	V_{ref} - 0.13V	V
I_{IH}	Input high leakage current[b]	No pulldown	–	2	µA
I_{IL}	Input low leakage current[c]	No pullup	-2	–	µA
I_{IHPD}	Input high leakage current[b,d]	With pulldown	40	200	µA
I_{ILPU}	Input low leakage current[c, d]	With pullup	-200	-40	µA
V_{OH}	High-level output voltage[d]	CMOS, at pin rated drive strength	0.9 · V_{DD_PX}	–	V
V_{OL}	Low-level output voltage[e]	CMOS, at pin rated drive strength	–	0.1 · V_{DD_PX}	V
I_{OZH}	Tri-state leakage current	Logic high output	–	1	µA
I_{OZL}	Tri-state leakage current	Logic low output	-1	–	µA

Table 9-13 Digital I/O characteristics for V_{DD_PX} = 1.2 V nominal (Continued)

Parameter		Comments	Min	Max	Unit
C_{IN}	Input capacitance[f]		1	2	pF
$C_{I/O}$	I/O capacitance[f]	I/O, DQS, DQ, or clock pins	1.25	2.5	pF

a. Pin voltage = V_{DD_PX}/2.
b. Pin voltage = GND and supply = V_{DD_PX} max.
c. Refer to Table 11-1 for pullup, pulldown, and keeper details.
d. Input and I/O capacitances are guaranteed by design, but are not 100% tested.
e. Refer to Table 11-1 for each output pin's drive strength (I_{OH} and I_{OL}); the drive strengths of many output pins are programmable and depend on the associated supply voltage
f. Input and I/O capacitances are guaranteed by design, but are not 100% tested.

Table 9-14 Digital I/O characteristics for VDD_PX = 2.85 V nominal (SD card interface)

Parameter		Comments	Min	Max	Unit
V_{IH}	High-level input voltage	CMOS/Schmitt	0.65·V_{DD_PX}	V_{DD_PX}+0.3	V
V_{IL}	Low-level input voltage	CMOS/Schmitt	-0.3	0.25·V_{DD_PX}	V
V_{SHYS}	Schmitt hysteresis voltage		100	–	mV
I_{IH}	Input high leakage current [a, b]	No pulldown	–	10	µA
I_{IL}	Input low leakage current [a, b]	No pullup	-10	–	µA
I_{IHPD}	Input high leakage current [a, c]	With pulldown	10	60	µA
I_{ILPU}	Input low leakage current [b, c]	With pullup	-60	-10	µA
I_{OZH}	Tri-state leakage current [a]	Logic high output, no pulldown	–	10	µA
I_{OZL}	Tri-state leakage current [b]	Logic low output, no pullup	-10	–	µA
I_{OZHPD}	Tri-state leakage current [a, c]	Logic high output with pulldown	10	60	µA
I_{OZHPU}	Tri-state leakage current [b, c]	Logic high output with pullup	-60	-10	µA
I_{OZHKP}	Tri-state leakage current [a, c]	Logic high output with keeper	-25	-5	µA
I_{OZLKP}	Tri-state leakage current [b, c]	Logic low output with keeper	5	25	µA
V_{OH}	High-level output voltage [d]	CMOS, at pin rated drive strength	V_{DD_PX} - 0.45	V_{DD_PX}	V
V_{OL}	Low-level output voltage [d]	CMOS, at pin rated drive strength	0	0.45	V
C_{IN}	Input capacitance [e]		–	5	pF

a. Pin voltage = V_{DD_PX} max. For keeper pins, pin voltage = V_{DD_PX} max - 0.45 V.
b. Pin voltage = GND and supply = V_{DD_PX} max. For keeper pins, pin voltage = 0.45 V and supply = V_{DD_PX} max.
c. Refer to Table 11-1 for pullup, pulldown, and keeper details.
d. Refer to Table 11-1 for each output pin's drive strength (I_{OH} and I_{OL}); the drive strengths of many output pins are programmable and depend on the associated supply voltage.
e. Input capacitance is guaranteed by design but is not 100% tested.

In all digital I/O cases, V_{OL} and V_{OH} are linear functions (Figure 9-4) with respect to the drive current (see Table 11-1). They can be calculated using these relationships:

$$Vol\,[\max] = \frac{\%\,drive \times 450}{100} mV$$

$$Voh\,[\min] = Vdd\_px - \left(\frac{\%\,drive \times 450}{100}\right) mV$$

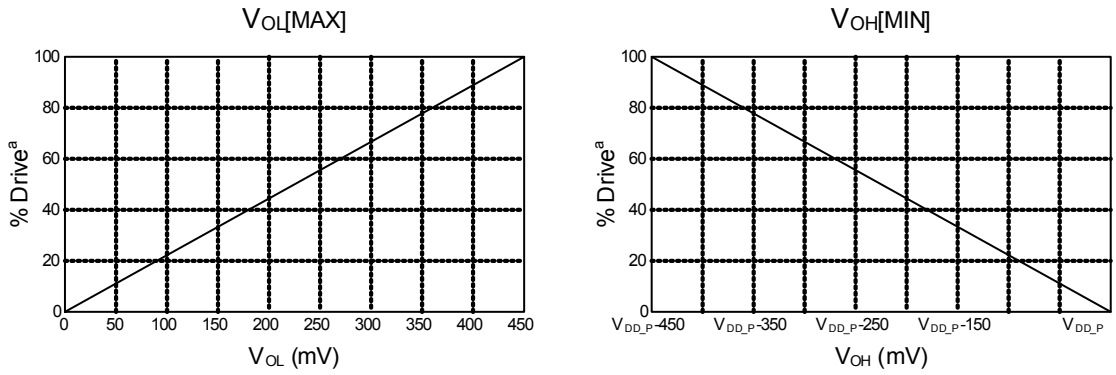

Figure 9-4 IV curve for VOL and VOH (valid for all VDD_PX)

9.5.4 Timing characteristics

Specifications for the device timing characteristics are included (where appropriate) under each function's section, along with all its other performance specifications. Some general comments about timing characteristics are included here.

NOTE All APQ8064 devices are characterized with actively terminated loads, so all baseband timing parameters in this document assume no bus loading. This is described further in Section 9.5.4.2.

9.5.4.1 Timing diagram conventions

The conventions used throughout this document for timing diagrams are shown in Figure 9-5. For each signal in the diagram:

- One clock period (T) extends from one rising clock edge to the next rising clock edge.
- The high level represents 1, the low level represents 0, and the middle level represents the floating (high-impedance) state.
- When both the high and low levels are shown, the meaning depends on the signal.
- A single signal indicates *don't care*.
- In the case of bus activity, if both high and low levels are shown, this indicates that the processor or external interface is driving a value, but that this value may or may not be valid.

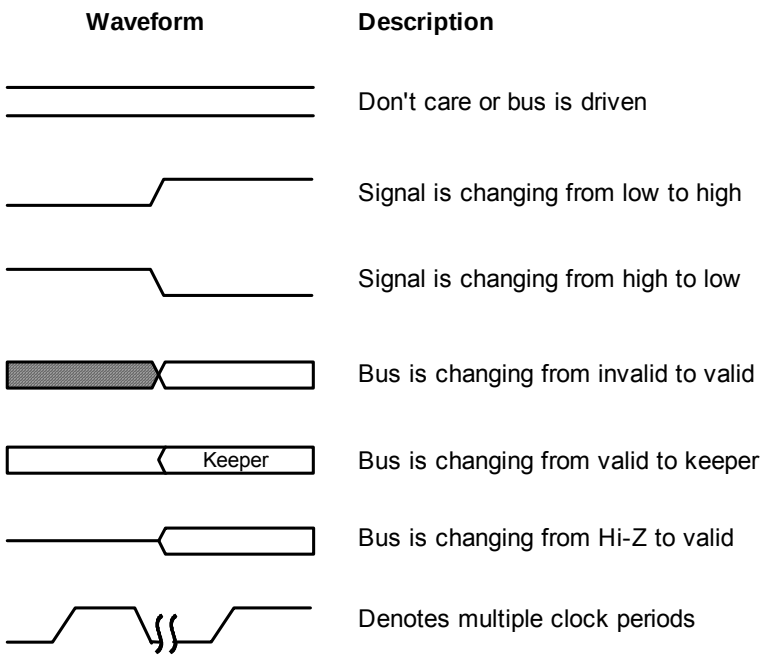

Figure 9-5 Timing diagram conventions

9.5.4.2 Rise and fall time specifications

The testers that characterize APQ8064 have actively terminated loads, making the rise and fall times quicker (mimicking a no-load condition). The impact that different external load conditions have on rise and fall times is shown in Figure 9-6.

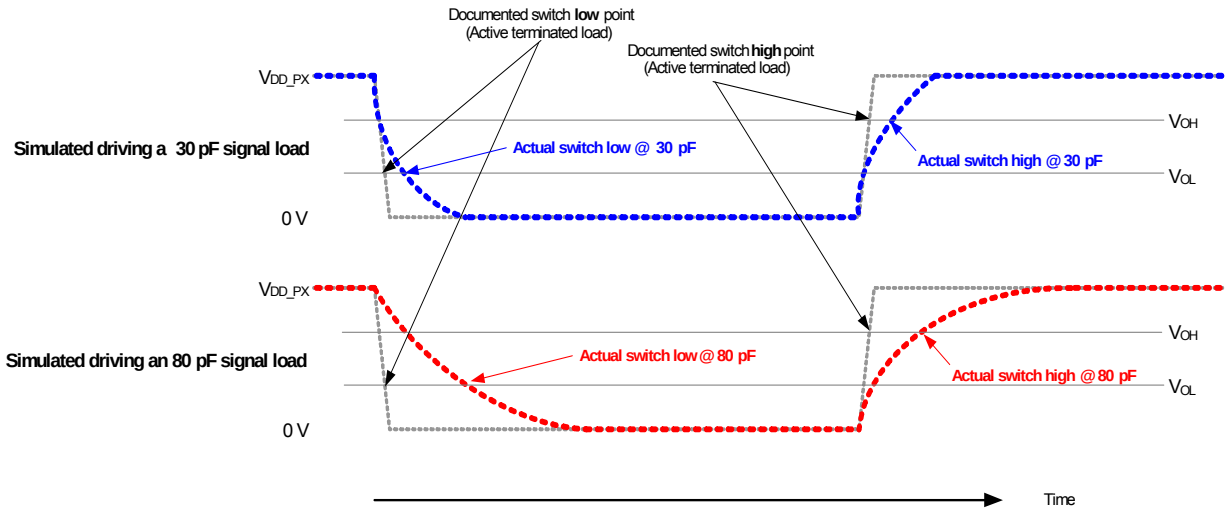

Figure 9-6 Rise and fall times under different load conditions

9.5.5 Memory support

NOTE Information contained in this section is preliminary and is subject to change.

9.5.5.1 EBI0 and EBI1

All timing parameters in this document assume no bus loading. Rise/fall times must be factored into the numbers in this document. For example, setup times will get worse and hold times may get better.

9.5.5.1.1 Pad drive strengths

Pads for EBI0/EBI1 are tailored for the 1.2 V interface and are source-terminated. Before the source termination, the pad drive strength is 15 mA to 60 mA. But at the pads, after the source termination, the drive strength at IOL, IOH is equivalent to 1.3 mA to 5.15 mA for PCDDR3 configuration in non-linear steps when the JEDEC standard range (90% to 10%) is followed.

9.5.5.2 PCDDR3 SDRAM on EBI1

This information will be included in future revisions of this document.

9.5.6 Multimedia

The multimedia functions supported by the APQ8064 that require external access (and therefore I/O specification) include:

- Camera interfaces
- Audio/visual (A/V) outputs
- Display support

Pertinent specifications for the associated I/Os are stated in the following subsections.

In addition, the APQ supports I^2S (Section 9.5.8.8) digital interface.

9.5.6.1 Camera interfaces

9.5.6.1.1 4-lane MIPI_CSI

Table 9-15 Summary of 4-lane MIPI_CSI support

Applicable standard	Feature exceptions	APQ variations
MIPI Alliance Specification v1.00 for camera serial interface	None	None

9.5.6.1.2 2-lane MIPI_CSI

Table 9-16 Summary of 2-lane MIPI_CSI support

Applicable standard	Feature exceptions	APQ variations
MIPI Alliance Specification v1.00 for camera serial interface	None	None

9.5.6.2 A/V outputs

9.5.6.3 HDMI

Table 9-17 Summary of HDMI support

Applicable standard	Feature exceptions	APQ variations
HDMI specification ver.1.4a	None	None

9.5.7 Display support

9.5.7.1 4-lane MIPI_DSI

Table 9-18 Summary of 4-lane MIPI_DSI support

Applicable standard	Feature exceptions	APQ8064 variations
MIPI Alliance specification v1.00 for camera serial interface	None	None

9.5.7.2 LVDS

Table 9-19 Summary of 4LVDS support

Applicable standard	Feature exceptions	APQ8064 variations
This information will be included in future revisions of this document.		

9.5.8 Connectivity

The connectivity functions supported by the APQ8064 include:

- High-speed USB port with built-in PHY and full-speed USB port (for USB-UICC only)
- Serial ATA (SATA) port
- PCI Express (PCIe) port
- Universal asynchronous receiver transmitter (UART) serial ports
- User identity module (UIM) ports
- Secure digital card controller (SDCC) ports
- Inter-integrated circuit (I^2C) interfaces for peripheral devices
- Inter-IC sound (I^2S) interfaces for digital audio support
- Serial peripheral interface (SPI) ports
- Pulse code modulation (PCM) port
- Transport stream interface (TSIF) ports

Pertinent specifications for these functions — where appropriate — are stated in the following subsections.

NOTE The following interfaces are multiplexed to output pins by properly configuring the seven generic serial bus interface (GSBI) ports: UART, UIM, I^2C, and SPI.

In addition to the following hardware specifications, consult the latest software release notes for software-based performance features or limitations.

9.5.8.1 USB interfaces

Table 9-20 Summary of USB support

Applicable standard	Feature exceptions	APQ variations
Universal Serial Bus Specification, Revision 2.0 (April 27, 2000 or later)	None	Operating voltages, system clock, and VBUS – see Table 9-21

Table 9-21 APQ-specific USBPHY specifications

Parameter	Comments	Min	Typ	Max	Unit
Supply voltages					
Dual-supply (see Table 8-1 for specifications)					
VDD_USBPHY_1P8 pin		1.73	1.80	1.87	V
VDD_USBPHY_3P3 pin		2.97	3.30	3.63	V
USBPHY_SYSCLK					
Frequency	19.2 MHz clock is required.	–	19.2	–	MHz
Clock deviation		-400	–	400	ppm
Jitter (peak-to-peak)	0.5 to 1.75 MHz	0	–	60	psec
Duty cycle		40	–	60	%
Low-level input voltage (V_{IL})		–	–	0.6	V
High-level input voltage (V_{IH})		1.27	–	–	V
USBPHY_VBUS					
Valid USB_HS_VBUS detection voltage		2.0	–	5.25	V

9.0.0.0.0.1 HSIC interfaces

Table 9-22 Summary of HSIC interface support

Applicable standard	Feature exceptions	APQ variations
High-Speed Inter-Chip USB Electrical Specification, Version 1.0 (a supplement to the USB 2.0 specification)	Device mode not supported.	None

9.5.8.2 SATA interface

Table 9-23 Summary of SATA support

Applicable standard	Feature exceptions	APQ variations
SATA Specification, Revision 1.0	None	None

9.5.8.3 PCIe interface

Table 9-24 Summary of PCIe support

Applicable standard	Feature exceptions	APQ variations
PCI Express Specification, Revision 2.0 (January 15, 2007 or later)	None	None

9.5.8.4 High-speed UART interface

Table 9-25 Summary of UART support

Applicable standard	Feature exceptions	APQ variations
EIA RS232-C	None	None

9.5.8.5 UIM interface

Table 9-26 Summary of UIM support

Applicable standard	Feature exceptions	APQ variations
ISO/IEC 7816-3	None	None

9.5.8.6 Secure digital card controller interfaces

Table 9-27 Summary of SDCC support

Applicable standard	Feature exceptions	APQ variations
Multi Media Card Host Specification version 4.4.1 and 4.5	None	Timing specifications – see Figure 9-7 and Figure 9-8.
Secure Digital: Physical Layer Specification version 3.0	None	
SDIO Card Specification version 3.0	None	

Single Data Rate - SDR

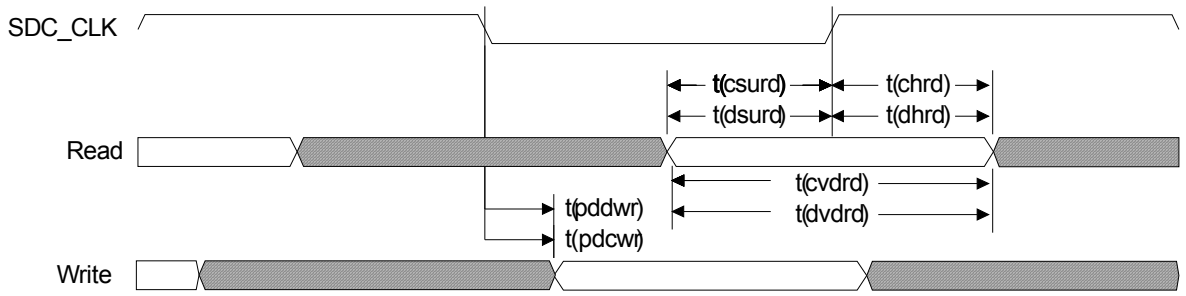

Figure 9-7 SDCC SDR timing waveforms

Double Data Rate - DDR

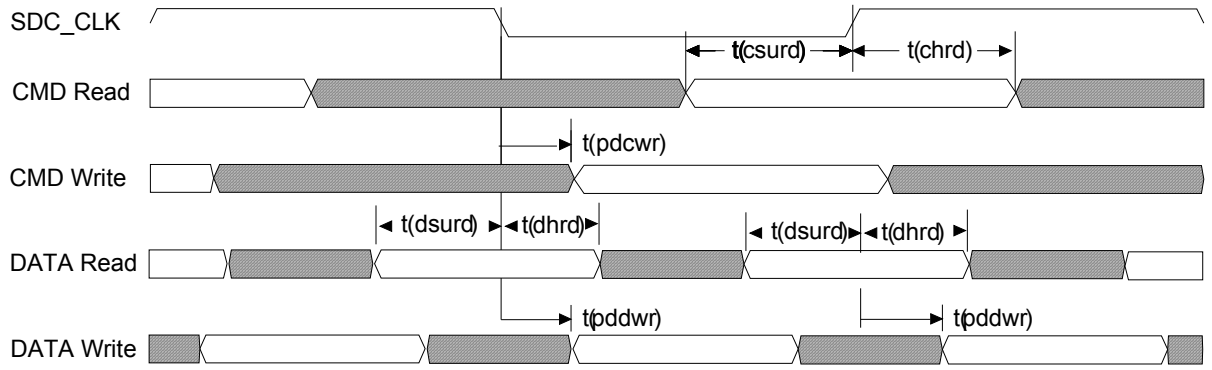

Figure 9-8 SDCC DDR timing waveforms

Table 9-28 SDC1/SDC3 DDR mode timing parameters[a]

Parameter		Min	Max	Unit
t(chrd)	Command hold	1.5	–	ns
t(csurd)	Command setup	6.3	–	ns
t(dhrd)	Data hold	1.5	–	ns
t(dsurd)	Data setup	2	–	ns
t(pddwr)	Propagation delay on data write	0.8	6	ns
t(pdcwr)	Propagation delay on command write	-8.2	3	ns

a. SDC1 and SDC3 DDR mode timing parameters are for clock frequencies up to 52 MHz.

Table 9-29 SDC1 SDR mode timing parameters[a]

Parameter		Min	Max	Unit
t(chrd)	Command hold	1.50	–	ns
t(csurd)	Command setup	2.50	–	ns

Table 9-29 SDC1 SDR mode timing parameters[a] (Continued)

Parameter		Min	Max	Unit
t(dhrd)	Data hold	1.50	–	ns
t(dsurd)	Data setup	2.50	–	ns
t(pddwr)	Propagation delay on data write	-3.7	1.50	ns
t(pdcwr)	Propagation delay on command write	-3.7	1.50	ns

a. SDC1 SDR timing parameters is for the clock frequencies up to 104 MHz.

Table 9-30 SDC1/SDC3 SDR104 mode timing parameters[a]

Parameter		Min	Max	Unit
t(cvdrd)	Command valid	2.50	–	ns
t(dvdrd)	Data valid	2.50	–	ns
t(pddwr)	Propagation delay on data write	-1.45	0.85	ns
t(pdcwr)	Propagation delay on command write	-1.45	0.85	ns

a. SDC1/SDC3 SDR104 mode timing parameters are for the clock frequencies up to 208 MHz.

Table 9-31 SDC2/SDC5 SDR33 mode timing parameters[a]

Parameter		Min	Max	Unit
t(chrd)	Command hold	1.50	–	ns
t(csurd)	Command setup	7.65	–	ns
t(dhrd)	Data hold	1.50	–	ns
t(dsurd)	Data setup	7.65	–	ns
t(pddwr)	Propagation delay on data write	-6.0	3.82	ns
t(pdcwr)	Propagation delay on command write	-6.0	3.82	ns

a. SDC2/SDC4 SDR33 mode timing parameters are for the clock frequencies up to 66 MHz.

9.5.8.7 I²C interface

Table 9-32 Summary of I²C support

Applicable standard	Feature exceptions	APQ variations
I²C Specification, version 2.1, January 2000 (Philips Semiconductor® document number 9398 393 40011)	■ High-speed mode (3.4 Mbps) is not supported. ■ 10-bit addressing is not supported. ■ Fast mode plus (1 Mbps) is not supported.	None

9.5.8.8 I²S interface

The APQ8064 has five separate I²S interfaces:

- Multichannel I²S (MI²S)
- Codec microphone I²S

- Secondary microphone I^2S
- Codec speaker I^2S
- Secondary speaker I^2S

All five I^2S interfaces meet the timing given in this section.

Table 9-33 Supported I^2S standards and exceptions

Applicable standard	Feature exceptions	APQ8064 variations
Philips Semiconductor, *I^2S Bus Specification*, revised June 5, 1996		The APQ8064 meets or exceeds this standard. The only exception is the APQ8064 requires a 45/55 duty cycle when the SCK clock source is from an external source

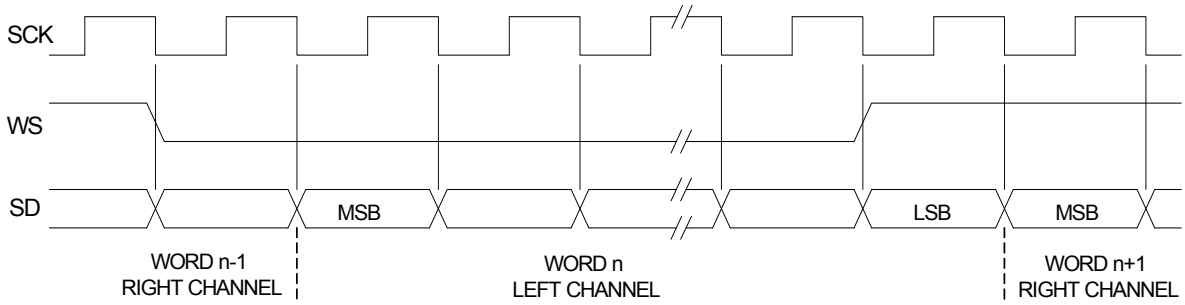

Figure 9-9 I^2S interface basic timing

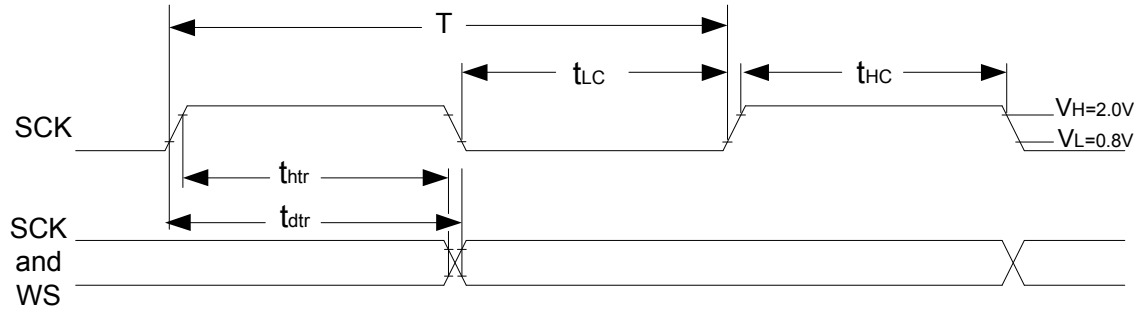

Figure 9-10 I^2S interface transmitter timing

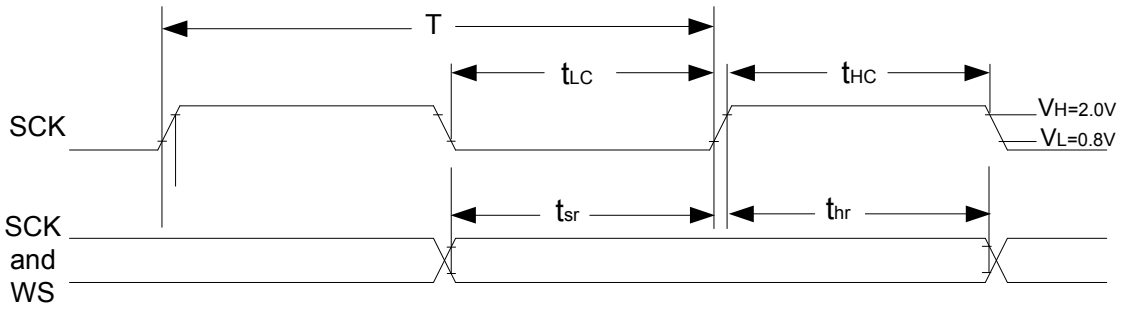

Figure 9-11 I²S interface receiver timing

Table 9-34 I²S interface timing using internal SCK clock

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Clock SCK						
Frequency	f	0		12.288	MHz	C_L = 10 pF - 40 pF
Clock period	T	0		81.38	ns	C_L = 10 pF - 40 pF
Clock high	t_{HC}	0.45T		0.55T	ns	C_L = 10 pF - 40 pF
Clock low	t_{LC}	0.45T		0.55T	ns	C_L = 10 pF - 40 pF
Inputs SD*, WS						
Setup time	t_{sr}	16.276	–	–	ns	
Hold time	t_{hr}	0	–	–	ns	
Outputs SD*, WS						
Delay	t_{dtr}	–	–	65.1	ns	C_L = 10 pF - 40 pF
Hold time	t_{htr}	0	–	–	ns	C_L = 10 pF - 40 pF

Table 9-35 I²S interface timing using external SCK clock

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Clock SCK						
Frequency	f	0		12.288	MHz	C_L = 10 pF - 40 pF
Clock period	T	0		81.38	ns	C_L = 10 pF - 40 pF
Clock high	t_{HC}	0.45T		0.55T	ns	C_L = 10 pF - 40 pF
Clock low	t_{LC}	0.45T		0.55T	ns	C_L = 10 pF - 40 pF
Inputs SD*, WS						
Setup time	t_{sr}	16.27	–	–	ns	
Hold time	t_{hr}	0	–	–	ns	
Outputs SD*, WS						
Delay	t_{dtr}	–	–	65.1	ns	C_L = 10 pF - 40 pF
Hold time	t_{htr}	0	–	–	ns	C_L = 10 pF - 40 pF

9.5.8.9 Serial peripheral interface (master only)

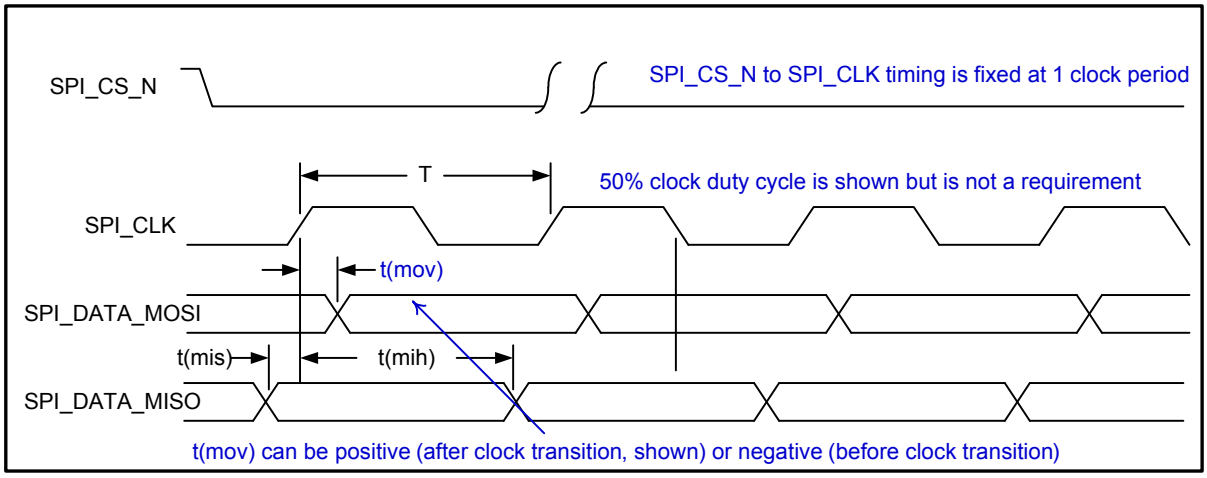

Figure 9-12 SPI master timing diagram

Table 9-36 SPI master timing characteristics (52 MHz max)

Parameter	Comments	Min	Typ	Max	Unit
SPI clock frequency		–	–	52	MHz
T (SPI clock period)		19.0	–	–	ns
t(ch)	Clock high	8.65	–	–	ns
t(cl)	Clock low	8.65	–	–	ns
t(mov)	Master output valid	-5	–	5	ns
t(mis)	Master input setup	5	–	–	ns
t(mih)	Master input hold	1	–	–	ns

9.5.8.10 Transport stream interfaces

Table 9-37 Summary of TSIF support

Applicable standard	Feature exceptions	APQ variations
ITU-T H.222.0 Transport Stream (HTS); also known as ISO/IEC 13818-1	None	None

Table 9-38 Transport stream timing characteristics (96 MHz max)

Parameter	Comments	Min	Typ	Max	Unit
TSIF (clock frequency)		–	–	96	MHz
t(hddata)	Data hold	0.1	–	–	ns
t(hden)	Data enable hold	0.1	–	–	ns
t(hdsync)	Data sync hold	0.1	–	–	ns

Table 9-38 Transport stream timing characteristics (96 MHz max) (Continued)

Parameter	Comments	Min	Typ	Max	Unit
t(sudata)	Data setup	4	–	–	ns
t(suenable)	Data enable setup	4	–	–	ns
t(susync)	Data sync setup	4	–	–	ns

9.5.9 Internal functions

Some internal functions require external interfaces to enable their operation. These include clock generation, modes and resets, and JTAG functions – as specified in the following subsections.

9.5.9.1 Clocks

Clocks that are specific to particular functions are addressed in the corresponding sections of this document. Others are specified here.

9.5.9.1.1 19.2 MHz core XO input

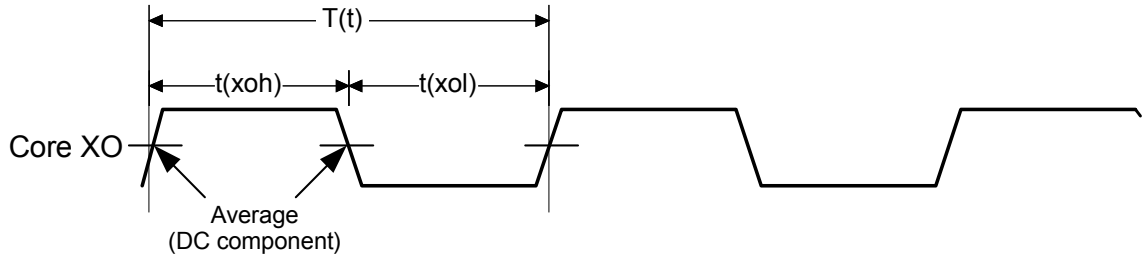

Figure 9-13 Core XO timing parameters

Table 9-39 Core XO timing parameters

Parameter		Comments	Min	Typ	Max	Unit
t(xoh)	Core XO logic high		22.6	–	29.5	ns
t(xol)	Core XO logic low		22.6	–	29.5	ns
T(t)	Core XO clock period		–	52.083	–	ns
1/T(t)	Frequency	19.2 MHz must be used.	–	19.2	–	MHz

9.5.9.1.2 Sleep clock

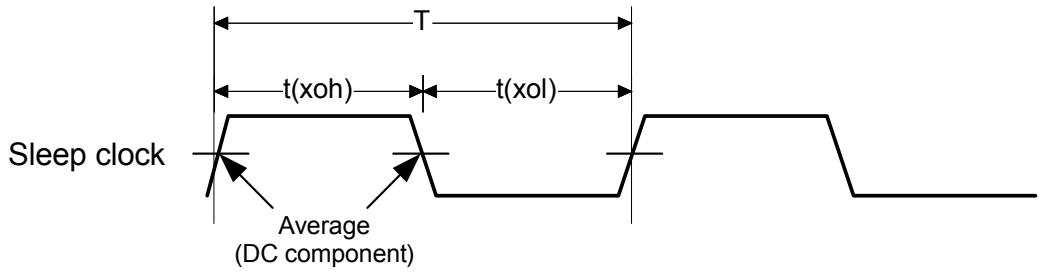

Figure 9-14 Sleep-clock timing parameters

Table 9-40 Sleep-clock timing parameters

Parameter		Comments	Min	Typ	Max	Unit
t(xoh)	Sleep-clock logic high		4.58	–	25.94	µs
t(xol)	Sleep-clock logic low		4.58	–	25.94	µs
T(t)	Sleep-clock period		–	30.518	–	µs
1/T(t)	Frequency		–	32.768	–	kHz

9.5.9.1.3 PXO (27 MHz) crystal oscillator

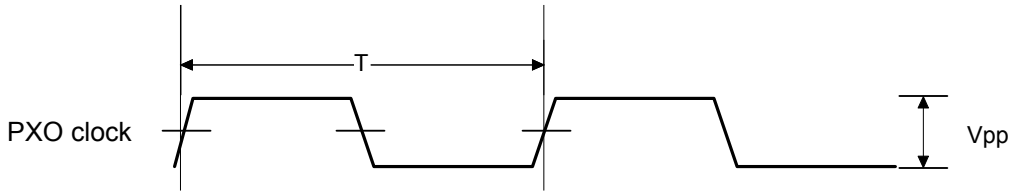

Figure 9-15 PXO (27 MHz) crystal oscillator timing parameters

Parameters for the 27 MHz crystal oscillator are listed in Table 9-41.

Table 9-41 PXO (27 MHz) crystal oscillator parameters

Parameter	Min	Typ	Max	Unit
Frequency	–	27	–	MHz
Frequency tolerance	-30	–	30	ppm
Series resistance (ESR)	–	–	60	Ω
Load capacitance	11	15	17	pF
Shunt capacitance	–	–	5	pF

9.5.9.2 Modes and resets

The mode and reset functions are basic digital I/Os that meet the performance specifications presented in Section 9.5.3.

9.5.9.3 JTAG

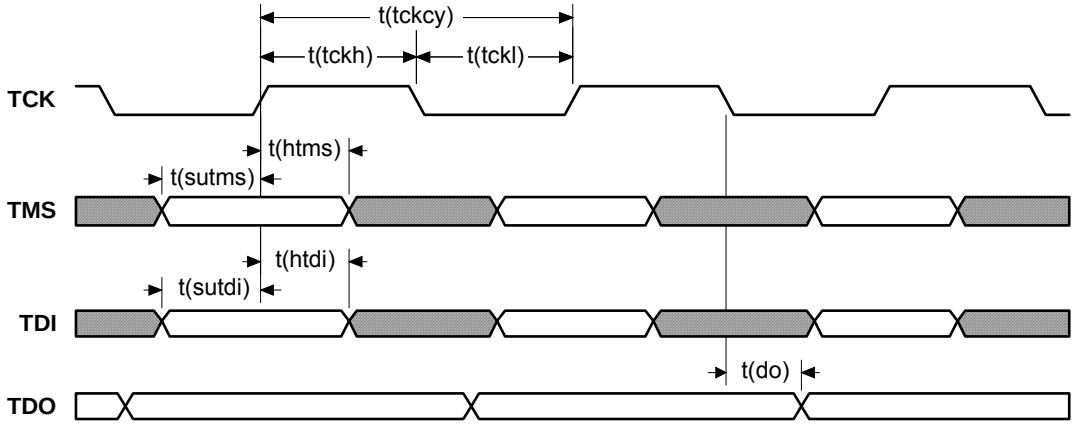

Figure 9-16 JTAG interface timing diagram

Table 9-42 JTAG interface timing characteristics

Parameter		Comments	Min	Typ	Max	Unit
t(tckcy)	TCK period		100	–	–	ns
t(tckh)	TCK pulse width high		40	–	–	ns
t(tckl)	TCK pulse width low		40	–	–	ns
t(sutms)	TMS input setup time		25	–	–	ns
t(htms)	TMS input hold time		25	–	–	ns
t(sutdi)	TDI input setup time		25	–	–	ns
t(htdi)	TDI input hold time		25	–	–	ns
t(do)	TDO data-output delay		–	–	70	ns

10 Clocks and Oscillators

10.1 System clocks

The PMIC includes several clock circuits whose outputs are used for general housekeeping functions, and elsewhere within the embedded computing system. These circuits include a 19.2 MHz XO with multiple controllers and buffers, an MP3 clock output, 32.768 kHz crystal support, an RC oscillator, sleep clock outputs, and internal SMPL and SMPS clocks. Performance specifications for these functions are presented Section 9.1.2.

10.2 LPASS clocks

- The LPASS PLL circuit is within the APQ's clock generation and distribution block.
- The LPASS clock controller (LCC) generates all the clocks needed for APQ audio functions, including the new SLIMbus and digital microphone interfaces.

10.2.1 Primary clock configuration

- The platform crystal oscillator (PXO, 27 MHz) is the reference source.
- The LPASS PLL output is routed to the LPASS, and selected as the LCC input signal.
- The LCC generates all audio clocks.
- Individual audio interfaces route the clocks to their functional blocks.
- Each interface allows an external clock source to be used, and allows the generated clock to be routed externally.

10.3 WCD clocks

- The APQ8064 IC LPASS clock controller provides the WCD IC clocks.
- A low-power RC oscillator circuit is used when the MCLK signal is off (when MBHC, aux PGA, and charge pumpblocks are in their standby modes).
- RC oscillator characteristics
  - 12.288 MHz nominal.
  - Frequency accuracy is improved by using an on-chip RC tuner.
  - A clean power source is generated by an on-chip LDO powered by VDD_DIG_IO.
  - Maximum supply current is 70 µA

Table 10-1 WCD clocks

Name	Clock source	Frequency	Comments
Active mode			
System clock	APQ8064 IC MCLK	12.288 MHz	WCD IC also supports 9.6, 24.576, and 19.2 MHz MCLK.
Tx ADC clock	MCLK / 2	6.144 MHz	
Rx DAC clock	MCLK / 2	6.144 MHz	
DMIC clock	MCLK / 4... or... / 6	3.072... or... 2.048 MHz	
SLIMbus clock	APQ IC LPASS	24.576 MHz	
Standby mode			
System clock	RC oscillator	12.288 MHz	Generated within the WCD IC, and only used by features that are on when MCLK from the MPQ IC is off.
MBHC	RC oscillator	12.288 MHz	
AUX_PGA	RC oscillator	12.288 MHz	
Charge pump	RC oscillator	12.288 MHz	

10.4 19.2 MHz core XO input

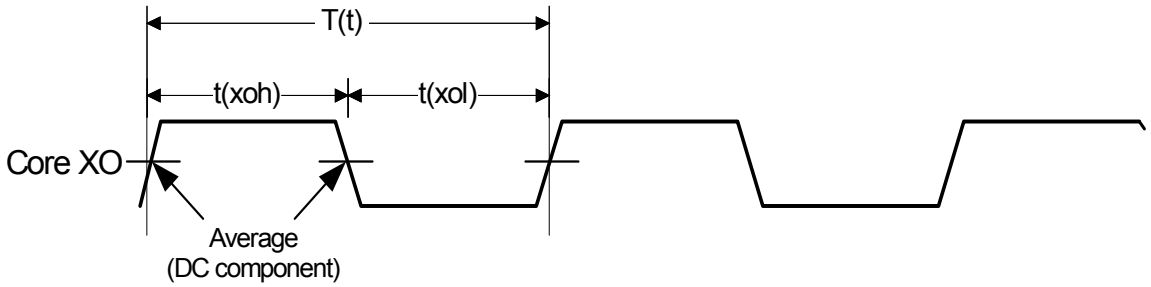

Figure 10-1 19.2 MHz Core XO timing parameters

Table 10-2 19.2 MHz Core XO timing parameters

Parameter		Comments	Min	Typ	Max	Unit
t(xoh)	Core XO logic high		22.6	–	29.5	ns
t(xol)	Core XO logic low		22.6	–	29.5	ns
T(t)	Core XO clock period		–	52.083	–	ns
1/T(t)	Frequency	19.2 MHz must be used.	–	19.2	–	MHz

10.5 48 MHz core VO input

Information will be included in future revisions of this document.

10.6 Sleep clock

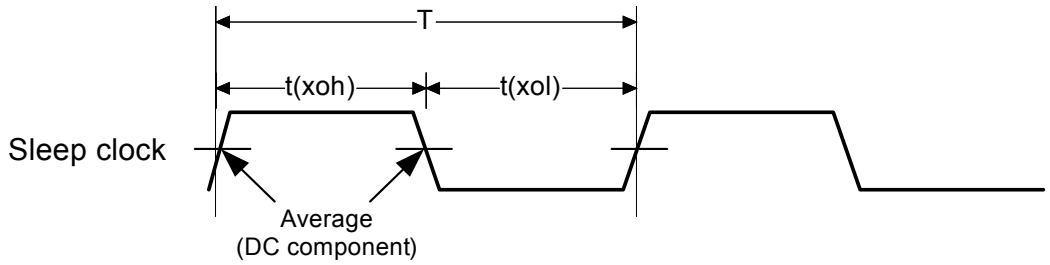

Figure 10-2 Sleep-clock timing parameters

Table 10-3 Sleep-clock timing parameters

Parameter		Comments	Min	Typ	Max	Unit
t(xoh)	Sleep-clock logic high		4.58	–	25.94	µs
t(xol)	Sleep-clock logic low		4.58	–	25.94	µs
T(t)	Sleep-clock period		–	30.518	–	µs
1/T(t)	Frequency		–	32.768	–	kHz

10.7 PXO (27 MHz) crystal oscillator

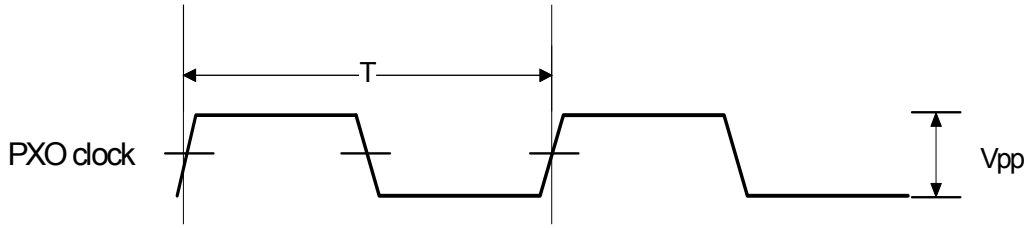

Figure 10-3 PXO (27 MHz) crystal oscillator timing parameters

Table 10-4 PXO (27 MHz) crystal oscillator parameters

Parameter	Min	Typ	Max	Unit
Frequency	-	27	-	MHz
Frequency tolerance	-30	–	30	ppm
Series resistance (ESR)	–	–	60	Ω
Load capacitance	11	15	17	pF
Shunt capacitance	-	-	5	pF

10.8 Source oscillators and external clock connections

GP_CLK outputs – direct clock signal

GP_MN output – M/N:D counter output signal

GP_PDM outputs – pulse density modulated (PDM) signal with the following configuration options:

- Input source: PXO or CXO; without dividing (or with divide-by-4)
- Enable/disable
- Output polarity
- Pulse density (number of output high counts versus low counts)

Table 10-5 Clock summary

Clock	Frequency	Usage
CXO – core crystal oscillator	19.2 MHz	Optional reference for LPASS, GSS, WCSS, and HSIC PLLs
PXO – platform crystal oscillator	27 MHz	Reference for all other PLLs
SLEEP_CLK – sleep clock	32.768 MHz	Reference during sleep mode

10.8.1 Clock regimes

See Section 6.3.4.

10.9 Power management

10.9.1 Resource and power manager (RPM)

Main RPM objective: lower the IC's average power consumption – static (1) and dynamic (2)

1. Static power management (primarily to limit leakage current)
   - Avoids using the high-powered processor
   - Executes code exclusively from internal RAM
   - Enables reduced logic supply of 0.5 V
2. Dynamic power management
   - Rapidly configures shared system resources and power-level configurations without impacting active processes and workloads.
   - Achieves optimal clock rate and supply voltage settings according to workload.
   - Improves overall system power efficiency while maintaining quality-of-service.
   - Minimizes overhead and latency needed to make voltage and clock change decisions.

10.9.1.1 Key RPM features

- Fast response times, low latency – less than 1 ms for clock frequency requests, 10 ms for supply voltage requests
- Autonomous and coordinated controls
  - Adjusts frequency, voltage, and resource usage without impacting other subsystems
  - Controls shared resources without other subsystems being active
  - Supports voting mechanisms for resource management
- Security – RPM is trusted at all times
  - Authenticates and validates trust level of subsystems calling RPM
  - Employs QFPROM
  - The Krait applications processor is assumed to be the secure root-of-trust (SROT) after initial boot
- Performs initial boot, coordinates other subsystems' boot-ups
- Resources controlled include: power management; clock sources and routing (CXO, PXO, sleep); supply voltages; clock frequencies; temperature compensation; and elements of the other APQ subsystems

10.9.1.2 RPM system operation

- Highly flexible microprocessor-based engine
  - Algorithms can be modified to achieve optimal power efficiency over a product's range of concurrent operations.
  - Facilitates security features like memory protection and safely sharing resources with nonsecure processors (LPA, QDSP6, etc.).
- System's sleep controller
  - Puts other subsystems into various sleep states to reduce leakage currents.
  - Upon wakeup, resources are enabled as needed to meet the requested operations, and base security levels are restored (effectively a warm boot).
- Optimizes system performance
  - Dynamic clock and voltage scaling for shared clocks and voltage domains minimizes power dissipation.
  - Arbitrates requests from all subsystems for shared resources like CXO, PXO, supply voltages, PLLs, memory, peripherals, and clocks for better efficiency.
  - Enables, disables, and/or scales shared resources on demand.
  - Intelligent power management using data from processors, resources, and applications, plus reports from performance, temperature, and process monitors

10.9.2 Input power management overview

Internal power management for both PMIC devices is controlled by the PM8921 IC. Features supported include:

- Dual-charger support
  - Fully integrated 30 V USB over-voltage protection
  - 30 V wall charger OVP (external OVP FET required)
- Valid external supply attachment and removal detection
- SMBC for better efficiency than linear charging
  - Four regulation control loops: USB input current, DC_IN input voltage, VPH_PWR output voltage, and battery current
- Supports lithium-ion and lithium-ion polymer
- Automated charging modes that allow PMIC battery charging with less software intervention
- Trickle, constant current, and constant voltage charging of the main battery
- ATC LED supply; supplements ATC current driver
- An expanded battery monitoring system (BMS) that includes a battery fuel gauge for accurate management of battery resources
- External battery MOSFET is optional
- Supports coin cell backup battery or keep-alive capacitor (including charging)
- Battery voltage alarms with programmable thresholds
- VDD collapse protection
- Under-voltage lockout (UVLO) protection
- Automated recovery from sudden momentary power loss (SMPL)

10.9.3 Output power management overview

PM8921 device

- Seven buck (step-down) switched-mode power supply circuits
  - Five high-frequency (HF-SMPS) circuits rated for 1.5 A each
  - Two fast transient (FT-SMPS) circuits rated for 2 A each
- 20 low-dropout regulator circuits with programmable output voltages, supporting a wide range of current ratings: 1.2 A (5), 600 mA (2), 300 mA (4), 150 mA (7), and 50 mA (2); in addition, there are two low-noise low-dropout (LDO) regulators for the clock system of which one is internal only.
- Seven low-voltage switches and two medium voltage switches for power supply gating to external circuits
  - Soft-start feature reduces in-rush current and avoids voltage drops at the source regulator
  - Over-current protection

- Supports dynamic voltage scaling (DVS) on key regulators
- Regulators can be individually enabled/disabled for power savings
- Low-power mode available on all regulators
- All regulated outputs are derived from a common bandgap reference and trimmed for ±1% accuracy

PM8821 device

- Two FT-SMPS circuits; rated for 2000 mA each
  - Static voltage scaling (SVS) – APQ open-loop control of FT-SMPS output voltage
  - Adaptive voltage scaling (AVS) – APQ closed-loop control of FT-SMPS output voltage to optimize processor supply voltage for power consumption vs. performance trade-offs
  - SMPS step control (SSC) – algorithm that manages voltage transitions between AVS set points to ensure a smooth, controlled ramp
- One internal low dropout regulator circuit to power up internal voltages; 50 mA
  - Low-power mode available on regulator
- All regulated outputs are derived from a common bandgap reference and trimmed for ±1% accuracy

11 GPIO

See Table 6-5 for I/O description (pad type) parameters.

NOTE GPIO pins can support multiple functions. To assign GPIOs to particular functions (such as the options listed in the table above), designers must identify all their application's requirements and map each GPIO to its function – carefully avoiding conflicts in GPIO assignments. Refer to Table 11-1 for a list of all supported functions for each GPIO.

NOTE Users must examine each GPIO's external connection and programmed configuration, and take steps necessary to avoid excessive leakage current. Combinations of the following factors must be controlled properly:

- GPIO configuration
  - Input versus output
  - Pull-up or pull-down
- External connections
  - Unused inputs
  - Connections to high-impedance (tri-state) outputs
  - Connections to external devices that may not be attached

Table 11-1 APQ8064 pin descriptions – GPIO[a]

Pad #	Pad name	Configurable function	Pad volt.	Pad type	Functional description
H17	GPIO_89	 USB2_HSIC_DATA VFE_CAMIF_TIMER_3B	P4	B-PD:nppukp B DO	Configurable I/O HSIC data VFE camera I/F timer 3B; sync or async configurable
H15	GPIO_88	 USB2_HSIC_STROBE VFE_CAMIF_TIMER_4B	P4	BH-PD:nppukp B DO	Configurable I/O HSIC strobe VFE camera I/F timer 4B; sync or async configurable
W21	GPIO_87	 SATA_LED BOOT_CONFIG_0	P3	B-PD:nppukp DI DI	Configurable I/O SATA status LED Boot configuration bit 0 (depends upon security fuse state)
AD22	GPIO_86	 PCI_E_PWRFLT_N	P3	B-PD:nppukp DI	Configurable I/O PCIe power-fault indication
AF26	GPIO_85	 GSBI7_0 PCI_E_PWREN_N	P3	B-PD:nppukp B DI	Configurable I/O General SBI 7 bit 0; UART, UIM, SPI, or I^2C PCIe interface signal to power up/down the transceiver

Table 11-1 APQ8064 pin descriptions – GPIO[a] (Continued)

Pad #	Pad name	Configurable function	Pad volt.	Pad type	Functional description
Y20	GPIO_84	GSBI7_1 PCI_E_PRSNT_2_N	P3	BH-PD:nppukp B DO	Configurable I/O General SBI 7 bit 1; UART, UIM, SPI, or I2C PCIe interface power presence detection
AA21	GPIO_83	GSBI7_2 PCI_E_WAKE_N	P3	BH-PD:nppukp B DO	Configurable I/O General SBI 7 bit 2; UART, UIM, SPI, or I2C PCIe interface link reactivation
Y21	GPIO_82	GSBI7_3 PCI_E_RST_N	P3	B-PD:nppukp B DI	Configurable I/O General SBI 7 bit 3; UART, UIM, SPI, or I2C PCIe interface core reset
E3	GPIO_81	SSBI_EXT_GPS	P3	BH-PD:nppukp B	Configurable I/O Single-wire serial bus interface for external GPS
AE23	GPIO_80	GNSS_BLANKING	P3	B-PD:nppukp DO	Configurable I/O GNSS Rx blanking control
F23	GPIO_79	SSBI_PMIC2	P3	B-PD:nppukp B	Configurable I/O Single-wire serial bus interface for PMIC 2
C28	GPIO_78	PS_HOLD	P3	B-PD:nppukp DO	Configurable I/O Power-supply hold signal to PMIC
J21	GPIO_77	PMIC2_USR_INT_N	P3	BH-PU:nppukp DI	Configurable I/O User (nonsecure) apps µP interrupt request from PMIC2
F22	GPIO_76	PMIC2_SEC_INT_N	P3	BH-PU:nppukp DI	Configurable I/O Secure apps µP interrupt request from PMIC2
C26	GPIO_75		P3	BH-PU:nppukp	Configurable I/O
G23	GPIO_74	PMIC1_USR_INT_N	P3	BH-PU:nppukp DI	Configurable I/O User (nonsecure) apps µP interrupt request from PMIC1
C27	GPIO_73	PMIC1_SEC_INT_N	P3	BH-PU:nppukp DI	Configurable I/O Secure apps µP interrupt request from PMIC1
H12	GPIO_72	HDMI_HPLUG_DET	P3	BH-PD:nppukp DI	Configurable I/O HDMI hot plug detect
A4	GPIO_71	HDMI_DDC_DATA	P3	B-PU:nppukp B	Configurable I/O HDMI display data channel – data
C4	GPIO_70	HDMI_DDC_CLK	P3	B-PU:nppukp B	Configurable I/O HDMI display data channel – clock
A3	GPIO_69	HDMI_CEC	P3	B-PU:nppukp B	Configurable I/O HDMI consumer electronics control
Y2	GPIO_68	SDC4_CLK	P3	B-PD:nppukp DO	Configurable I/O Secure digital controller 4 clock
AC3	GPIO_67	SDC4_CMD	P3	B-PD:nppukp B	Configurable I/O Secure digital controller 4 command
AB3	GPIO_66	SDC4_DATA_0	P3	B-PD:nppukp B	Configurable I/O Secure digital controller 4 data bit 0
AB2	GPIO_65	SDC4_DATA_1	P3	BH-PD:nppukp B	Configurable I/O Secure digital controller 4 data bit 1
AB4	GPIO_64	SDC4_DATA_2	P3	B-PD:nppukp B	Configurable I/O Secure digital controller 4 data bit 2
AC2	GPIO_63	SDC4_DATA_3 SSBI_BT	P3	BH-PD:nppukp B B	Configurable I/O Secure digital controller 4 data bit 3 Single-wire serial bus interface for Bluetooth

Table 11-1 APQ8064 pin descriptions – GPIO[a] (Continued)

Pad #	Pad name	Configurable function	Pad volt.	Pad type	Functional description
D1	GPIO_62	 TSIF1_SYNC SDC2_DATA_0	P3	B-PD:nppukp DI B	Configurable I/O Transport stream interface 1 sync Secure digital controller 2 data bit 0
C6	GPIO_61	 TSIF2_DATA SDC2_DATA_1	P3	BH-PD:nppukp DI B	Configurable I/O Transport stream interface 2 data Secure digital controller 2 data bit 1
H8	GPIO_60	 TSIF2_EN SDC2_DATA_2	P3	B-PD:nppukp DI B	Configurable I/O Transport stream interface 2 enable Secure digital controller 2 data bit 2
H5	GPIO_59	 TSIF2_CLK SDC2_CLK	P3	B-PD:nppukp DI B	Configurable I/O Transport stream interface 2 clock Secure digital controller 2 clock
G6	GPIO_58	 TSIF2_SYNC SDC2_DATA_3	P3	BH-PD:nppukp DI B	Configurable I/O Transport stream interface 2 sync Secure digital controller 2 data bit 3
E1	GPIO_57	 TSIF1_DATA SDC2_CMD	P3	B-PD:nppukp DI B	Configurable I/O Transport stream interface 1 data Secure digital controller 2 command
H6	GPIO_56	 TSIF1_EN SPI_CS3A_N_GSBI1	P3	BH-PD:nppukp DI DO-Z	Configurable I/O Transport stream interface 1 enable Serial peripheral interface chip-select 3A for SPI on GSBI1
G5	GPIO_55	 TSIF1_CLK	P3	BH-PD:nppukp DI	Configurable I/O Transport stream interface 1 clock
U2	GPIO_54	 MIC_I2S_MCLK GSBI5_0 UICC_DM USB_FS1_SE0_A	P3	B-PD:nppukp DO B B B	Configurable I/O Secondary microphone codec I^2S master clock General SBI 5 bit 0; UART, UIM, SPI, or I^2C UICC data minus Full-speed USB SE0 for diagnostics
U1	GPIO_53	 MIC_I2S_WS GSBI5_1 UICC_DP USB_FS1_DAT_A	P3	B-PD:nppukp B B B B	Configurable I/O Secondary microphone codec I^2S word select (L/R) General SBI 5 bit 1; UART, UIM, SPI, or I^2C UICC data plus Full-speed USB data for diagnostics
V5	GPIO_52	 MIC_I2S_SCK GSBI5_2 USB_FS1_OE_A_N	P3	BH-PD:nppukp B B DO	Configurable I/O Secondary microphone codec I^2S bit clock General SBI 5 bit 2; UART, UIM, SPI, or I^2C Full-speed USB output enable for diagnostics
V4	GPIO_51	 MIC_I2S_DIN GSBI5_3 VFE_CAMIF_TIMER_6A	P3	B-PD:nppukp DI B DO	Configurable I/O Secondary microphone codec I^2S data input General SBI 5 bit 3; UART, UIM, SPI, or I^2C VFE camera I/F timer 6A; sync or async configurable
V3	GPIO_50	 SPKR_I2S_MCLK GP_CLK_1B BOOT_CONFIG_1	P3	BH-PD:nppukp DO DO DI	Configurable I/O Secondary speaker codec I^2S master clock General-purpose clock output 1B Boot configuration bit 1(depends upon security fuse state)
W2	GPIO_49	 SPKR_I2S_DOUT GP_PDM_2A	P3	BH-PD:nppukp DO DO	Configurable I/O Secondary speaker codec I^2S data output General-purpose PDM output 2A, 12-bit, clocked at XO/4

Table 11-1 APQ8064 pin descriptions – GPIO[a] (Continued)

Pad #	Pad name	Configurable function	Pad volt.	Pad type	Functional description
V1	GPIO_48	SPKR_I2S_WS SPI_CS2C_N_GSBI1	P3	B-PD:nppukp B DO-Z	Configurable I/O Secondary speaker codec I2S word select (L/R) Serial peripheral interface chip-select 2C for SPI on GSBI1
V7	GPIO_47	SPKR_I2S_SCK VFE_CAMIF_TIMER_7A	P3	BH-PD:nppukp B DO	Configurable I/O Secondary speaker codec I2S bit clock VFE camera I/F timer 7A; sync or async configurable
AB5	GPIO_46	AUDIO_PCM_CLK VFE_CAMIF_TIMER_5A	P3	B-PU:nppdkp B DO	Configurable I/O Audio PCM clock VFE camera I/F timer 5A; sync or async configurable
AA5	GPIO_45	AUDIO_PCM_SYNC VFE_CAM_TIMER_4A	P3	BH-PD:nppukp B DO	Configurable I/O Audio PCM sync VFE camera I/F timer 4A; sync or async configurable
AB1	GPIO_44	AUDIO_PCM_DIN GP_PDM_1B	P3	BH-PD:nppukp DI DO	Configurable I/O Audio PCM data input General-purpose PDM output 1B, 12-bit, clocked at XO/4
W1	GPIO_43	AUDIO_PCM_DOUT	P3	B-PD:nppukp DO-Z	Configurable I/O Audio PCM data output
V6	GPIO_42	CDC_SPKR_I2S_WS	P3	BH-PD:nppukp B	Configurable I/O Primary speaker codec I2S word select (L/R)
AD3	GPIO_41	CDC_SPKR_I2S_DOUT AUD_SB1_DATA_A	P3	BH-PD:nppukp DO B	Configurable I/O Primary speaker codec I2S data output Audio bidirectional data (A) via SLIMbus 1
AD2	GPIO_40	CDC_SPKR_I2S_SCK AUD_SB1_CLK_A	P3	B-PD:nppukp B B	Configurable I/O Primary speaker codec I2S bit clock Audio clock (A) via SLIMbus 1
AA6	GPIO_39	CDC_SPKR_I2S_MCLK AUD_SB1_MCLK BOOT_CONFIG_2	P3	BH-PD:nppukp DO DO DI	Configurable I/O Primary speaker codec I2S master clock Audio master clock for SLIMbus 1 Boot configuration bit 2 (depends on security fuse state)
B4	GPIO_38	CDC_MIC_I2S_DIN1 GP_PDM_0A USB_FS1_SE0_B	P3	BH-PD:nppukp DI DO B	Configurable I/O Primary microphone codec I2S data input 1 General-purpose PDM output 0A, 12-bit, clocked at XO/4 Full-speed USB SE0 for diagnostics
E5	GPIO_37	CDC_MIC_I2S_DIN0 USB_FS1_DAT_B	P3	B-PD:nppukp DI B	Configurable I/O Primary microphone codec I2S data input 0 Full-speed USB data for diagnostics
B5	GPIO_36	CDC_MIC_I2S_WS SPI_CS1C_N_GSBI1 USB_FS1_OE_B_N	P3	BH-PD:nppukp B DO-Z DO	Configurable I/O Primary microphone codec I2S word select (L/R) Serial peripheral interface chip-select 1C for SPI on GSBI1 Full-speed USB output enable for diagnostics
H10	GPIO_35	CDC_MIC_I2S_SCK	P3	B-PD:nppukp B	Configurable I/O Primary microphone codec I2S bit clock
B3	GPIO_34	CDC_MIC_I2S_MCLK GP_CLK_0B BOOT_CONFIG_3	P3	BH-PD:nppukp DO DO DI	Configurable I/O Primary microphone codec I2S master clock General-purpose clock output 0B Boot configuration bit 3 (depends on security fuse state)

Table 11-1 APQ8064 pin descriptions – GPIO[a] (Continued)

Pad #	Pad name	Configurable function	Pad volt.	Pad type	Functional description
AA1	GPIO_33	MI2S_MCLK GP_PDM_2B BOOT_CONFIG_4	P3	B-PD:nppukp B DO DI	Configurable I/O Multiple I2S interface master clock General-purpose PDM output 2B, 12-bit, clocked at XO/4 Boot configuration bit 4 (depends on security fuse state)
Y1	GPIO_32	MI2S_SD0 GP_CLK_2A	P3	BH-PD:nppukp B DO	Configurable I/O Multiple I2S interface serial data channel 0 General-purpose clock output 2A
AD1	GPIO_31	MI2S_SD1 AUD_SB1_CLK_B	P3	B-PD:nppukp B B	Configurable I/O Multiple I2S interface serial data channel 1 Audio clock (B) via SLIMbus 1
AC1	GPIO_30	MI2S_SD2 AUD_SB1_DATA_B	P3	BH-PD:nppukp B B	Configurable I/O Multiple I2S interface serial data channel 2 Audio bidirectional data (B) via SLIMbus 1
Y3	GPIO_29	MI2S_SD3	P3	BH-PD:nppukp B	Configurable I/O Multiple I2S interface serial data channel 3
Y6	GPIO_28	MI2S_SCK	P3	B-PD:nppukp B	Configurable I/O Multiple I2S interface bit clock
AA2	GPIO_27	MI2S_WS	P3	B-PD:nppukp B	Configurable I/O Multiple I2S interface word select (L/R)
AF24	GPIO_26	TS_PENIRQ_N	P3	BH-PU:nppukp DI	Configurable I/O Touch screen pen interrupt
AC22	GPIO_25	GSBI2_0 GP_CLK_2B	P3	B-PD:nppukp B DO	Configurable I/O General SBI 2 bit 0; UART, UIM, SPI, or I2C General-purpose clock output 2B
AC23	GPIO_24	GSBI2_1	P3	B-PD:nppukp B	Configurable I/O General SBI 2 bit 1; UART, UIM, SPI, or I2C
AD24	GPIO_23	GSBI2_2	P3	BH-PD:nppukp B	Configurable I/O General SBI 2 bit 2; UART, UIM, SPI, or I2C
AE21	GPIO_22	GSBI2_3 GP_PDM_1A	P3	BH-PD:nppukp B DO	Configurable I/O General SBI 2 bit 3; UART, UIM, SPI, or I2C General-purpose PDM output 1A, 12-bit, clocked at XO/4
AF23	GPIO_21	GSBI1_0	P3	B-PD:nppukp B	Configurable I/O General SBI 1 bit 0; UART, UIM, SPI, or I2C
AG26	GPIO_20	GSBI1_1	P3	B-PD:nppukp B	Configurable I/O General SBI 1 bit 1; UART, UIM, SPI, or I2C
AF27	GPIO_19	GSBI1_2 VFE_CAM_TIMER_5B	P3	BH-PD:nppukp B DO	Configurable I/O General SBI 1 bit 2; UART, UIM, SPI, or I2C VFE camera I/F timer 5B; sync or async configurable
AA20	GPIO_18	GSBI1_3 GP_PDM_0B VFE_CAM_TIMER_1B	P3	BH-PD:nppukp B DO DO	Configurable I/O General SBI 1 bit 3; UART, UIM, SPI, or I2C General-purpose PDM output 0B, 12-bit, clocked at XO/4 VFE camera I/F timer 1B; sync or async configurable
D3	GPIO_17	GSBI6_0 BT_DATA_STROBE	P3	B-PD:nppukp B B	Configurable I/O General SBI 6 bit 0; UART, UIM, SPI, or I2C Bluetooth dual-function signal – serial data and strobe
C3	GPIO_16	GSBI6_1 BT_CTL	P3	B-PD:nppukp B DO	Configurable I/O General SBI 6 bit 1; UART, UIM, SPI, or I2C Bluetooth control signal

Table 11-1 APQ8064 pin descriptions – GPIO[a] (Continued)

Pad #	Pad name	Configurable function	Pad volt.	Pad type	Functional description
F6	GPIO_15		P3	BH-PD:nppukp	Configurable I/O
		GSBI6_2		B	General SBI 6 bit 2; UART, UIM, SPI, or I2C
		FM_SDI		B	FM radio serial data interface
H9	GPIO_14		P3	B-PD:nppukp	Configurable I/O
		GSBI6_3		B	General SBI 6 bit 3; UART, UIM, SPI, or I2C
		SSBI_FM		B	Single-wire serial bus interface for FM radio
AF22	GPIO_13		P3	B-PD:nppukp	Configurable I/O
		GSBI4_0		B	General SBI 4 bit 0; UART, UIM, SPI, or I2C
AD25	GPIO_12		P3	B-PD:nppukp	Configurable I/O
		GSBI4_1		B	General SBI 4 bit 1; UART, UIM, SPI, or I2C
AF25	GPIO_11		P3	BH-PD:nppukp	Configurable I/O
		GSBI4_2		B	General SBI 4 bit 2; UART, UIM, SPI, or I2C
		MDP_VSYNC_E		B	MDP vertical sync – external
		VFE_CAM_TIMER_7C		DO	VFE camera I/F timer 7C; sync or async configurable
		SPI_CS2B_N_GSBI1		DO-Z	Serial peripheral interface chip-select 2B for SPI on GSBI1
AD26	GPIO_10		P3	BH-PD:nppukp	Configurable I/O
		GSBI4_3		B	General SBI 4 bit 3; UART, UIM, SPI, or I2C
		VFE_CAM_TIMER_6C		DO	VFE camera I/F timer 6C; sync or async configurable
		SPI_CS1B_N_GSBI1		DO-Z	Serial peripheral interface chip-select 1B for SPI on GSBI1
AD23	GPIO_9		P3	B-PD:nppukp	Configurable I/O
		GSBI3_0		B	General SBI 3 bit 0; UART, UIM, SPI, or I2C
AD21	GPIO_8		P3	B-PD:nppukp	Configurable I/O
		GSBI3_1		B	General SBI 3 bit 1; UART, UIM, SPI, or I2C
AE26	GPIO_7		P3	BH-PD:nppukp	Configurable I/O
		GSBI3_2		B	General SBI 3 bit 2; UART, UIM, SPI, or I2C
		TS_EOC		DI	Touch screen end-of-conversion
		SPI_CS1A_N_GSBI1		DO-Z	Serial peripheral interface chip-select 1A for SPI on GSBI1
		SPI_CS3B_N_GSBI1		DO-Z	Serial peripheral interface chip-select 3B for SPI on GSBI1
AC24	GPIO_6		P3	BH-PD:nppukp	Configurable I/O
		GSBI3_3		B	General SBI 3 bit 3; UART, UIM, SPI, or I2C
		GPS_PPS_OUT		DO	GPS one pulse per second output
		GPS_PPS_IN		DI	GPS one pulse per second input
		VFE_CAM_TIMER_4C		DO	VFE camera I/F timer 4C; sync or async configurable
		SPI_CS2A_N_GSBI1		DO-Z	Serial peripheral interface chip-select 2A for SPI on GSBI1
		SSBI_TS		B	Single-wire serial bus interface for touch screen
AG25	GPIO_5		P3	B-PD:nppukp	Configurable I/O
		CAM_MCLK0		DO	Camera master clock 0
		BOOT_CONFIG_5		DI	Boot configuration bit 5 (depends on security fuse state)
AG24	GPIO_4		P3	B-PD:nppukp	Configurable I/O
		VFE_CAM_TIMER_3A		DO	VFE camera I/F timer 3A; sync or async configurable
		CAM_MCLK1		DO	Camera master clock 1
		GP_CLK_1A		DO	General-purpose clock output 1A
		BOOT_CONFIG_6		DI	Boot configuration bit 6 (depends on security fuse state)
AE22	GPIO_3		P3	B-PD:nppukp	Configurable I/O
		VFE_CAM_TIMER_2		DO	VFE camera I/F timer 2; sync or async configurable
		GP_CLK_0A		DO	General-purpose clock output 0A
		WDOG_DISABLE		DI	Watchdog timer disable input

Table 11-1 APQ8064 pin descriptions – GPIO[a] (Continued)

Pad #	Pad name	Configurable function	Pad volt.	Pad type	Functional description
AG23	GPIO_2		P3	B-PD:nppukp	Configurable I/O
		VFE_CAM_TIMER_1A		DO	VFE camera I/F timer 1A; sync or async configurable
		GP_MN		DO	General-purpose M/N:D counter output
		CAM_MCLK2		DO	Camera master clock 2
		BOOT_FROM_ROM		DI	Boot configuration bit to select boot from ROM option
F7	GPIO_1		P3	B-PD:nppukp	Configurable I/O
		MDP_VSYNC_S		B	MDP vertical sync – secondary
		VFE_CAM_TIMER_7B		DO	VFE camera I/F timer 7B; sync or async configurable
E6	GPIO_0		P3	B-PD:nppukp	Configurable I/O
		MDP_VSYNC_P		B	MDP vertical sync – primary
		VFE_CAM_TIMER_6B		DO	VFE camera I/F timer 6B; sync or async configurable

a. Refer to Table 6-5 for parameter and acronym definitions.

NOTE Seven 4-pin sets of GPIOs are available as general serial bus interface (GSBI) ports that can be configured for UART, UIM, SPI, or I^2C operation. Detailed pin assignments are presented in Table 11-2 for each configuration.

Table 11-2 GSBI configurations [a b]

Option	Configuration	GSBI bit 3	GSBI bit 2	GSBI bit 1	GSBI bit 0
GSBI1 GPIO pins =		GPIO_18	GPIO_19	GPIO_20	GPIO_21
GSBI2 GPIO pins =		GPIO_22	GPIO_23	GPIO_24	GPIO_25
GSBI3 GPIO pins =		GPIO_6	GPIO_7	GPIO_8	GPIO_9
GSBI4 GPIO pins =		GPIO_10	GPIO_11	GPIO_12	GPIO_13
GSBI5 GPIO pins =		GPIO_51	GPIO_52	GPIO_53	GPIO_54
GSBI6 GPIO pins =		GPIO_14	GPIO_15	GPIO_16	GPIO_17
GSBI7 GPIO pins =		GPIO_82	GPIO_83	GPIO_84	GPIO_85
1	4-pin UART	UART_TX DO 4-pin UART transmit data	UART_RX DI 4-pin UART receive data	UART_CTS DI 4-pin UART clear-to-send	UART_RFR DO 4-pin UART ready-for-receive
2	4-pin SPI	SPI_DATA_MOSI B 4-pin SPI master out/slave in	SPI_DATA_MISO B 4-pin SPI master in/slave out	SPI_CS_N B 4-pin SPI chip select	SPI_CLK B 4-pin SPI clock
3	3-pin UIM + 1 GPIO	UIM_DATA B UIM data	UIM_CLK DO UIM clock	UIM_RESET_N DO UIM reset	GPIO_XX B Configurable I/O
4	2-pin I^2C + 2-pin UART	UART_TX DO 2-pin UART transmit data	UART_RX DI 2-pin UART receive data	I2C_SDA B I^2C serial data	I2C_SCL B I^2C serial clock
5	UIM + I^2C	UIM_DATA B UIM data	UIM_CLK DO UIM clock	I2C_SDA B I^2C serial data	I2C_SCL B I^2C serial clock
6	4 GPIOs	GPIO_XX B Configurable I/O	GPIO_XX B Configurable I/O	GPIO_XX B Configurable I/O	GPIO_XX B Configurable I/O

a. The three rows within cell entries are: 1) pad function, 2) pad type, and 3) functional description.

b. Client rate control interfaces (CRCI) allow a data mover (DM) client with limited memory space to throttle data flow. A given CRCI allows either the primary or the secondary device to access one DM at a time. SPI and UARTDM are GSBI interfaces that require DM access to achieve the higher throughput rates. I^2C, UART, UIM, etc., do not need a DM.

The design constraints on the GSBI assignment are 1) Two GSBI interfaces sharing the same CRCI cannot both access the DM at the same time. For example, GSBI4 and GSBI7 cannot both be configured as SPI or UARTDM, and still have access to the DM. 2) GSBI1, GSBI2, and GSBI3 cannot be assigned as SPI or UARTDM, since the crypto engine (CE) requires access to the DM to achieve the throughput requirement.

Table 11-3 Client rate control interface access

CRCI #	Primary (a)	Secondary (b)
1	CE_3_INB	TSIF2
2	CE_3_OTB	CE_1_INB
3	RESERVED (GND)	CE_1_OTB
4	RESERVED (GND)	CE_2_INB
5	GSBI_3_IN	CE_2_OTB
6	GSBI_3_OUT	GSBI_6_OUT
7	GSBI_4_IN	GSBI_7_IN
8	GSBI_4_OUT	GSBI_7_OUT
9	GSBI_5_IN	RESERVED (GND)
10	GSBI_5_OUT	RESERVED (GND)
11	GSBI_6_IN	TSIF1/TSIF2
12	GSBI_1_IN	RESERVED (GND)
13	GSBI_1_OUT	RESERVED (GND)
14	GSBI_2_IN	CE_3_INB
15	GSBI_2_OUT	CE_3_OTB

12 DDR Memory Controller and External Memory Interface

12.1 Memory controller

12.1.1 Key DDR memory controller features

- Supports DDR on address bus
- Two major clock domains (AXI slave and DDR controller)
- Multiple AXI-to-DDR clock modes
  - Synchronous (1:1), iso-synchronous (1:2), asynchronous
- Highly flexible with many configurable parameters, including interface timing
- Flexible memory page management with various page open/close policies
- Out-of-order command execution and read data return
- Multiple high-priority tiers for sophisticated handling of priority requests
- Dynamic clock frequency switching
- 512-byte write data buffer and 512-byte read data FIFO
- Embedded memory protection unit (XPU) guards against unauthorized access
- Sequential burst support; no interleave burst support
- Auto-refresh, temperature adjusted auto-refresh, posted auto-refresh, and self-timed refresh
- I/O calibration
- DIMs handle center-aligning of memory controls and data
- Performance monitors with event outputs to SPDM
- Powerdown and deep powerdown (DPD) support

12.2 External memory

12.2.1 EEPROM

For more information, refer to *EEPROM Software Configuration Data Table (CDT) Application Note* document.

12.3 MMC/SD

12.3.1 Secure Digital Controller

The APQ8064 IC provides up to four SD interfaces that provide the following features or functions.

- Clock output up to 104 MHz on SDC1/SDC2 and up to 208 MHz on SDC3; up to 67 MHz on the other interfaces
- 1.8 V/2.85 V dual-voltage operation on SDC3; 1.8 V operation on the other three
- Support for SDIO host mode
- SDIO compatible WLAN (802.11)
- Interface with SD/MMC memory cards up to 2 TB
- 10 k pull-up resistor on command pin; placeholder pull-ups are recommended on the data lines

Table 12-1 SDC

SDC	Function	Width	Maximum clock rate
SDC1	eMMC	8-bits	104 MHz SDR at 1.8 V 152 MHz DDR at 1.8 V
SDC2	Available	4-bits	104 MHz SDR at 1.8
SDC3	SD/MMC	4-bits	208 MHz SDR at 1.8 V 52 MHz DDR at 1.8 V
SDC4	Available	4-bits	52 MHz DDR at 1.8 V

12.4 PCDDR3 SDRAM on EBI1

This information will be included in future revisions of this document.

12.5 eMMC NAND flash on SDIO

- Fourth-generation SD card controller, known as SDCC4
- Supports eMMC and eSD devices; MMC v4.5 and SDIO v3.0
  - eMMC will be tested on in-house evaluation platforms

- Up to 104 MHz (SDR)
- Requires 10 k to 100 k pull-up resistors on DATA[7:0] and CMD signals
- Internal pull-up resistors can be used if power consumption and BOM count are concerns
  - Include placeholders for external pull-up resistors, to ensure compliance is met on a reference board design.

For more information, refer to *Multimedia Card/Secure Digital Card Application Note* document.

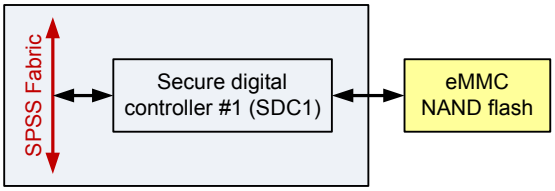

Figure 12-1 SDC1 and eMMC

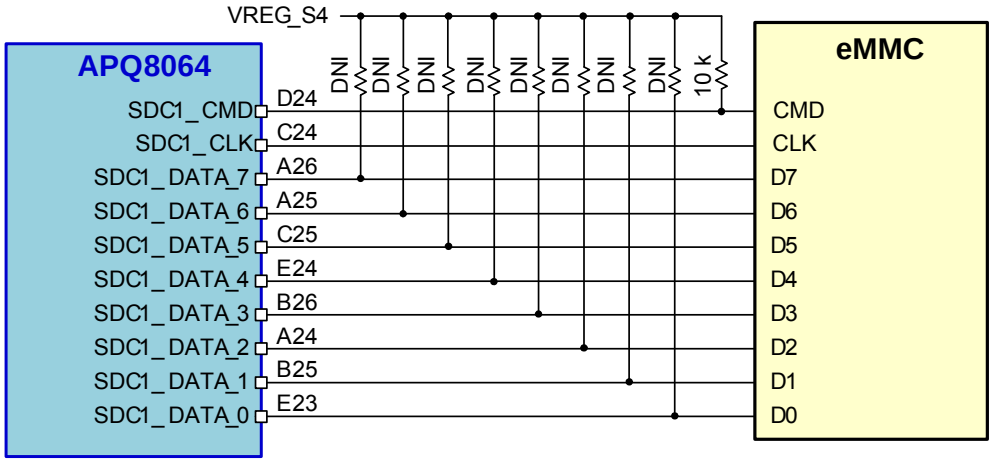

Figure 12-2 SDC1 high-level diagram

- The SDC1 port connects to an embedded NAND flash memory device.
  - 1.8 V interface (VREG_S4).
  - The memory device also requires 2.95 V (VREG_L5, not shown).
  - eMMC NAND via SDC1 is the primary boot device

See Section 9.5.8.6 for SDIO details.

13 Video Processing Subsystem

13.1 Display interfaces

Table 13-1 Display interfaces

Display interface	Target capabilities	Comment
4-lane MIPI DSI	Up to WQXGA (2048 × 1536), 24 bpp, 60 Hz refresh	Primary
LVDS	Up to WQXGA (2048 × 1536), 24 bpp, 60 Hz refresh	Alternate primary
4-lane MIPI DSI	Up to QHD (960 × 540), 24 bpp, 60 Hz refresh	Secondary
HDMI v1.4a w/HDCP	1080p, 60 Hz refresh	External (enable one at a time)
Concurrent dual display	2048 × 1536 (primary) + 960 × 540 (secondary)	
Processing support	Comment	
MDP 4.4	Latest version of fourth-generation mobile display processor hardware accelerator with support for 2048 × 1536 display resolution	

13.1.1 Example dual display

Table 13-2 Example dual display configurations

Example	Configuration
1	Primary panel using 4-lane DSI or LVDS + HDMI Tx; GUI on primary panel + 1080p video over HDMI
2	Primary panel using 4-lane DSI or LVDS + secondary panel using 4-lane DSI; Independent content on both displays (like video on one and GUI on other)

13.1.2 Camera sensor interfaces

Table 13-3 Camera interfaces

Parameter	Characteristic
Maximum sensor resolution	20 MP
Sensor input rate	228 MHz
Sensor pixel depth	8/10/12 bits per pixel
Supported input formats	Bayer RGB YCbCr 4:2:2 interleaved 12-8, 12-6, 10-8, 10-6 MIPI compression 8/10/12 MIPI raw

Table 13-3 Camera interfaces

Parameter	Characteristic
3D camera support	8 MP per channel (left & right)
Web camera support	8 MP

13.1.3 MDP

MDP is the latest version of fourth-generation mobile display processor hardware.accelerator with support for 2048 × 1536 display resolution. Figure 13-1 shows a high-level diagram.

- Dedicated accelerator hardware for transferring updated images from memory to display interfaces
- While the MDP transfers an image, it performs a final set of operations to that image
- Reduces circuit redundancy, offloads ARM and aDSP, improves system efficiency, and saves DC power

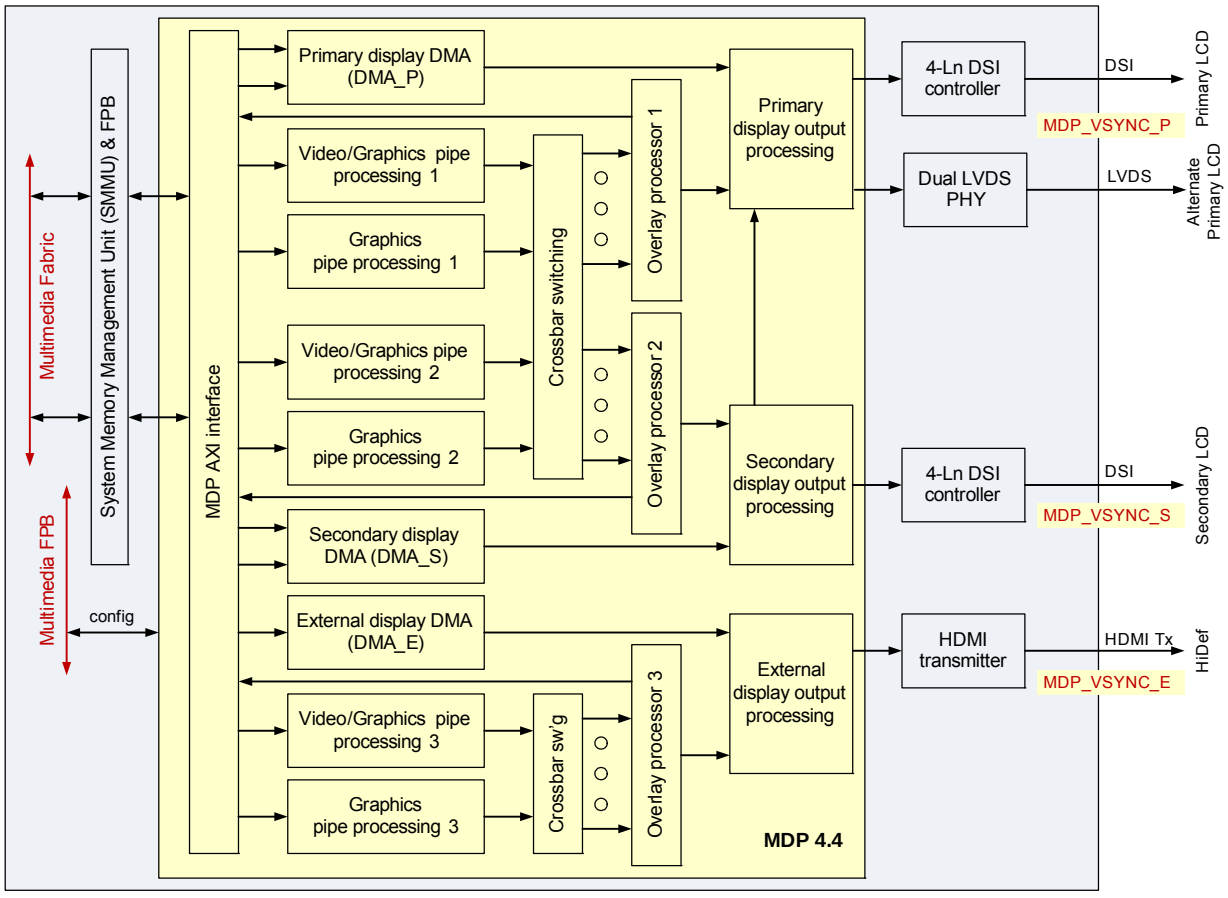

Figure 13-1 MDP high-level diagram

Table 13-4 Key MDP 4.4 features

Feature	Description
Graphics layer	
Input format	8/16/24-bit alpha RGB
Max resolution	2048 × 1536 LVDS or DSI; 1920 × 1200 other interfaces
Scaling	1x/8 to 20x
Filtering	Horizontal and vertical
Bit-depth promotion	Source cropping
Source cropping	
Video layer	
Input format	1/2-plane YUV
Max resolution	1080p each layer
Scaling	1x/8 to 20x
Filtering	Horizontal and vertical
Source cropping	
De-interlacing	
Sharpening	
Histogram data collect	
Noise inject (dithering)	
Contrast enhancement	
Noise filtering	
Blending	
V / G layer alignment	Arbitrary
Blend order constraints	None
Color keying	Video and graphics
Layer allocation for dual displays	4 layers, each can be allocated to primary or secondary display
Pre-multiplied alpha support	
LCD processing	
Integrated LCD controller	
HW cursor support (64 x 64 max)	
Gamma correction	
Up to 24 bits per pixel	
Color correction	
Dithering	

Table 13-4 Key MDP 4.4 features (Continued)

Feature	Description
Histogram data collection	
HW-based ABL for power savings	
Background color	

13.1.4 MIPI Display Serial Interfaces

- Display serial interfaces
  - Per Mobile Industry Processor Interface (MIPI) specification
  - One high-speed clock lane and one to four data lanes
  - Low-voltage differential signaling (LVDS)
  - PHY block provides physical interface to display device
- DSI transmitter features
  - MIPI DSI specification version 1.01
  - MIPI D-PHY specification versions 0.65, 0.81, and 0.90
  - Video and command modes
    - Four data lanes, up to four virtual channels
  - Up to 1 Gbps per lane high-speed mode bandwidth
  - Video color depths
    - 24-bpp RGB888
    - 18-bpp RGB666 loose or packed
    - 16-bpp RGB565

14 USB

14.1 Supported applications

- Peripheral mode
  - Mass storage
  - MTP for music and video content transfers
  - CDC/OBEX for NMEA and diagnostic
  - CDC/ECM for data services
  - SICD for PictBridge
- Host mode
  - HID supporting keyboard
  - Mouse and gamepad controller connectivity
  - Mass storage supporting USB flash drive and HDD connectivity

14.2 USB interfaces

Table 14-1 Summary of USB support

Applicable standard	Feature exceptions	APQ variations
Universal Serial Bus Specification, Revision 2.0 (April 27, 2000 or later)	None	Operating voltages, system clock, and VBUS – see Table 14-2

Table 14-2 APQ-specific specifications

Parameter	Comments	Min	Typ	Max	Unit
Supply voltages					
Dual-supply (see Table 8-1 for specifications)					
VDD_USBPHY_1P8 pin		1.73	1.80	1.87	V
VDD_USBPHY_3P3 pin		2.97	3.30	3.63	V
USBPHY_SYSCLK					
Frequency	19.2 MHz clock is required.	–	19.2	–	MHz
Clock deviation		-400	–	400	ppm
Jitter (peak-to-peak)	0.5 to 1.75 MHz	0	–	60	ppm

Table 14-2 APQ-specific specifications (Continued)

Parameter	Comments	Min	Typ	Max	Unit
Duty cycle		40	–	60	%
Low-level input voltage (V_{IL})		–	–	0.6	V
High-level input voltage (V_{IH})		1.27	–	–	V
USBPHY_VBUS					
Valid USB_HS_VBUS detection voltage		2.0	–	5.25	V

14.2.1 HSIC interfaces

Table 14-3 Summary of HSIC interface support

Applicable standard	Feature exceptions	APQ variations
High-speed Inter-chip USB Electrical Specification, version 1.0; (a supplement to the USB 2.0 specification – see Section 14.2.1)	Device-mode not supported	None

15 GSBI

GSBI pin details were provided in Chapter 11 – GPIO.

15.1 GSBI features

- 7 general serial bus interface (GSBI) ports are available
- Each is four bits wide – GSBIxx_[3:0]
- Each GSBI can support the following serial bus protocols
  - UART
  - UIM
  - SPI
  - I2C
- GSBIs are distributed throughout subsystems

15.2 UART features

The UART_DM is used to support high-speed UART operation up to 4 Mbps and medium data-rate IrDA operation up to 1.152 Mbps.

Advantages of the UART_DM block include:

- Rate-controlled data mover with separate CRCI channels for Rx and Tx
- 256 byte Rx and Tx FIFOs
- Access to the fast peripheral bus (32-bit wide AHB interface) rather than the slow bus
- Maintains traditional level interrupts directly to the microprocessor when the data mover is not available

Note that the UART_DM Tx and Rx channels are similar to the basic UART channels, except that the FIFOs are implemented in SRAM and the FIFO controls and IRQ generation are in the DM controller block.

15.3 UIM

15.3.1 UIM features

- Data rates up to 4 MHz
- Dual-voltage 1.8 or 2.85 V support
- PMIC level translation is required to support dual-voltage UIM modules

15.3.2 UIM initialization

The APQ device can recognize and initialize a UIM only during its powerup sequence, not during regular operation.

During a powerup sequence, whether a true powerup or a soft-reset, the UIM clock and data lines are active as they execute their initialization process one UIM slot at a time (if more than one is used). After initialization, the slots' operation depends upon whether a module is detected.

- If a module is detected:
  - The data line stays active, even if data is not being transmitted (between accesses). It maintains its marking state (logic high) between accesses.
  - The clock is only active during accesses; it is turned off between accesses to save power. The state of the clock when off is programmable, and must be selected to support the module's characteristics.
  - Even though the clock is turned off between accesses, the interface is still active. The data, reset, and power lines all remain high (assuming an active-low reset).
  - Note that the interface stays on once the module is detected, even during APQ sleep modes; the current consumption continues.
- If a module is not detected (module not inserted or not recognized, broken connection, etc.):
  - The interface is deactivated.
  - All lines are low and there is no chance to operate or communicate with a module until the next powerup sequence.

15.4 I^2C features

- Two-wire bus for inter-IC communications supporting any IC fabrication process
  - Each device is recognized by a unique address and can operate as either a transmitter or receiver, depending upon the device function.
- The I^2C controller provides an interface between the CPSS fast peripheral bus (FPB), an advanced high-performance bus (AHB), and the industry standard I^2C serial bus
  - Handles the I^2C protocol and frees up the on-chip processor (and AHB) to handle other operations
  - It is I^2C-compliant, high-speed mode (HS-mode)-compliant, and a master-only device

- I^2C pins use GPIOs configured as open-drain outputs; the pull-up resistor is provided by the slave
- Camera auto-focus control via I^2C originates with the aDSP; a separate hardware request port is required at the I^2C controller.

15.5 SPI

15.5.1 SPI features

- 4-bit synchronous serial data link
- Master mode supported
- Up to 52 MHz in master mode
- Master device initiates data transfers; multiple slave devices are supported by using chip-selects
- No explicit communication framing, error checking, or defined data word lengths, so the transfers are strictly at the “raw” bit level

15.5.2 SPI protocol requirements

1. As an SPI master, the core supports several SPI system configurations, including 1 through 5 and multimaster.
2. As an SPI master, the core supports SPI_CS0_N, SPI_CS1_N, SPI_CS2_N, and SPI_CS3_N.
3. As an SPI master, the core supports SPI_CLK.
4. As an SPI master, when no transfers are taking place (IDLE), the core supports SPI_CLK_IDLE_LOW and SPI_CLK_IDLE_HIGH.
5. As an SPI master, the core supports leaving the SPI_CLK running when no SPI_CS#_N is asserted (during IDLE).
6. As an SPI master, the core supports SPI_MOSI tri-state during IDLE (optional).
7. As an SPI master, the core supports Input_First_Mode.
8. As an SPI master, the core supports Output_First_Mode.
9. As an SPI master, the core supports any value of N between 4 and 32.
10. As an SPI master or slave, the core supports the following half-duplex modes (MDM is master-only):
    a. SPI_MOSI only with SPI_MISO held low
    b. SPI_MISO only with SPI_MOSI held low
    c. Half-duplex on a bidirectional signal (defined for system configuration 3 only).

11. As an SPI master, the core supports a mechanism to control the number of SPI_CLK ticks between the assertion of different SPI_CS signals. Even though there is no formal flow control mechanism, a slave may require dead time between SPI_CS assertions – this capability meets that potential requirement.
12. As an SPI master, the core supports the SPI_CS_N master requirements.
13. As an SPI master, the core supports assertion of SPI_CS#_N between each transfer of size N (CS is normally de-asserted). As an option, SPI_CS#_N can be asserted for a “first transfer” and left asserted for T transfers through the “last transfer” T. Under this option, requirement #11 above still applies, but the SPI_CLK is turned off every N bits while SPI_CS#_N is left asserted. This corresponds to the multitransfer chip-select (MX_CS).
14. As an SPI master, the core supports configuring SPI_CS#_N as active high (optional).

15.0.1 Master only

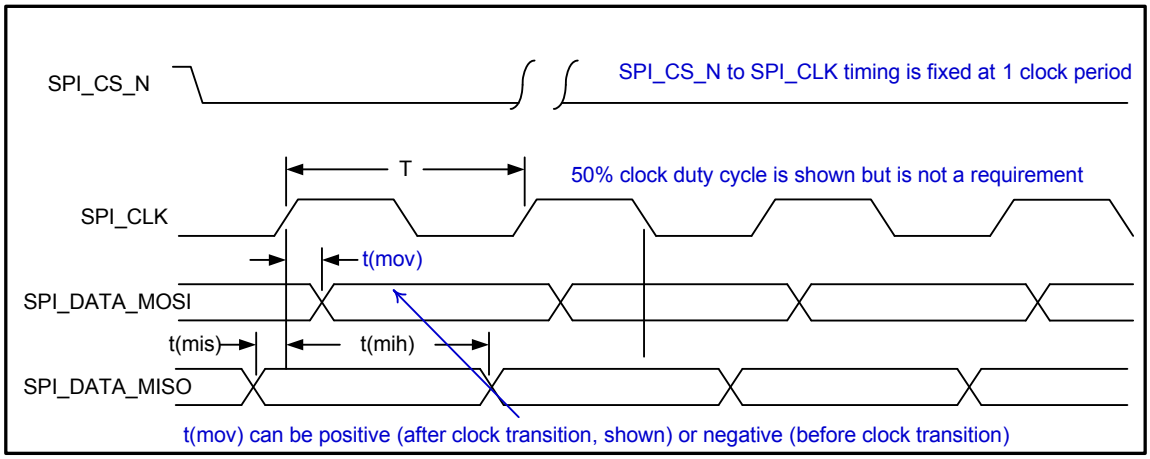

Figure 15-1 SPI master timing diagram

Table 15-1 SPI master timing characteristics (52 MHz max)

Parameter	Comments	Min	Typ	Max	Unit
SPI clock frequency		–	–	52	MHz
T (SPI clock period)		19.0	–	–	ns
t(ch)	Clock high	8.65	–	–	ns
t(cl)	Clock low	8.65	–	–	ns
t(mov)	Master output valid	-5	–	5	ns
t(mis)	Master input setup	5	–	–	ns
t(mih)	Master input hold	1	–	–	ns

16 Audio Interface

Two 2-pin SLIMbus interfaces and I^2S/I^2C bus are provided for audio and sensor usage.

The audio codec supports two control modes:

- MIPI SLIMbus: Data and control on the same data line
- I^2S/I^2C: Control over I^2C and data over I^2S

The SLIMbus core manages the SLIMbus (Serial Low-power Inter-chip Media Bus) audio interface. The SLIMbus comply with MIPI alliance Specification for Serial Low-power Interchip Media Bus Version 1.01.01.

16.1 SLIMbus

- Two-wire, multi-drop interface that supports a wide range of digital audio and control solutions for mobile terminals
- Defined by the MIPI Alliance
- External framer mode not supported

16.1.1 SLIMbus features

- Audio, data, and control on single bus
- Lower pin count
- Supports 10+ components at typical bus lengths and speeds
- Supports multiple high-quality audio channels
- Multiple concurrent sample rates on one bus
- Efficient peer-to-peer communications
- Standardized message set
- Improved software reuse
- Increased interoperability
- Dynamic clock rates for optimizing power
- Maximum SLIMbus clock = 28.8 MHz

16.2 I²S

The APQ8064 I²S interface supports external audio devices.

Table 16-1 MI²S for HDMI 7.1 Surround Sound

Parameter	Performance	Comments
I²S master or slave	Both	
Sample rates	8, 16, 24, 32, 48, 96 kHz	
Clock rates	64·Fs,128·Fs,256·Fs	Audio playback example: MCLK is typically 256·48 kHZ = 12.228 MHz
Channel support	Stereo	
Resolution	16, 24, 32 bits	
Duplex support	Full duplex	

17 Motor Control

The PMIC supports silent incoming call alarms with its vibration motor driver. The vibration driver is a programmable voltage output that is referenced to V_{DD}; when off, its output voltage is V_{DD}. The motor is connected between V_{DD} and the VIB_DRV_N pin.

Performance specifications for the vibration motor driver circuit are listed in Table 17-1.

Table 17-1 Vibration motor driver performance specifications

Parameter	Comments	Min	Typ	Max	Units
Output voltage (V_m) error[a]	V_{DD} > 3.2 V; I_m = 0 to 175 mA;				
Relative error	V_m setting = 1.2 to 3.1 V	-6	–	+6	%
Absolute error	Total error = relative + absolute	-60	–	+60	mV
Headroom[b]	I_m = 175 mA	–	–	200	mV
Short circuit current	VIB_DRV_N = V_{DD}	225	–	600	mA

a. The vibration motor driver circuit is a low-side driver. The motor is connected directly to VDD, and the voltage across the motor is $V_m = V_{DD} - V_{out}$, where V_{out} is the PMIC voltage at VIB_DRV_N.

b. Adjust the programmed voltage until the lowest motor voltage occurs while still meeting the voltage accuracy specification. This lowest motor voltage ($V_m = V_{DD} - V_{out}$) is the headroom.

Some vibration motor features are:

- Vibration motor driver programmable from 1.2 to 3.1 V in 100 mV increments
- Programmable voltage output referenced to V_{DD}
- When off, its output voltage is V_{DD}
- Motor connected between V_{DD} and VIB_DRV_N
- Voltage across motor is $V_m = V_{DD} - V_{out}$
- V_{out} is the voltage at the PMIC pin.

18 Keypad

The PMIC hardware supports key press detection. The GPIOs can be configured to implement a keypad interface supporting a matrix of up to 18 rows by 8 columns. Performance specifications that are specific to the keypad interface are listed in Table 18-1.

Table 18-1 Keypad interface performance specifications

Parameter	Comments	Min	Typ	Max	Units
Supply voltage		–	1.8	–	V
Load capacitance		–	–	100	pF
Sense lines					
Pull-up current		20.8	31.5	42.2	µA
Pull-down current		400	600	800	µA
Key-stuck delay	Number of 32 kHz cycles = 325,000	7.94	9.92	13.60	sec
Drive lines					
Drive strength	Open-drain outputs	–	0.6	–	mA

19 Analog-to-Digital Converter

19.1 General housekeeping features

- ADC input switches and analog multiplexing selects from several possible inputs (including MPPs)
- Input scaling increases the effective ADC resolution
- On-chip HK/XO ADC for HK functions
- ADC controller to arbitrate multiple simultaneous conversion requests
- 19.2 MHz VCTCXO support
- Five 19.2 MHz TCXO outputs with independent controllers
  - Three analog (low-noise) and two digital (low-power) outputs
- HS-USB support with 19.2 MHz reference clock output
- MP3 support with 2.4 MHz clock output (low power)
- 32.768 kHz sleep crystal support
- On-chip 19.2 MHz RC oscillator for backup
- Oscillator detectors and automated switch-over
- One dedicated sleep clock output plus configurable GPIOs for two more
- Real-time clock for tracking time and generating associated alarms
- On-chip adjustments minimize crystal oscillator frequency errors
- Over-temperature protection (smart thermal control)
- Buffered VREF outputs via configurable MPPs

19.2 Analog multiplexer and scaling circuits

A set of analog switches, analog multiplexers, and voltage scaling circuits select and condition a single analog signal for routing to the on-chip HK/XO ADC. The multiplexer and scaling functions are summarized in Table 19-1.

Table 19-1 Analog multiplexer and scaling functions

Ch #	Description	Typical input range (V)	Scaling	Typical output range (V)
0	VCOIN pin[a]	2.0 to 3.25	1/3	0.67 to 1.08
1	VBAT pin	2.5 to 4.5	1/3	0.83 to 1.5

Table 19-1 Analog multiplexer and scaling functions (Continued)

Ch #	Description	Typical input range (V)	Scaling	Typical output range (V)
2	OVP_SNS pin (over-voltage protected)[b]	4.5 to 9.5	1/6	0.75 to 1.58
3	–	–	–	–
4	VPH_PWR[a]	2.5 to 4.5	1/3	0.83 to 1.5
5	IBAT: battery charge current	0.3 to 1.5	1	0.3 to 1.5
6	Selected input from MPP[c]	0.1 to (VDDA - 0.1)	1	0.1 to (VDDA - 0.1)
7	Selected input from MPP[c]	0.3 to 3*(VDDA - 0.1)	1/3	0.1 to (VDDA - 0.1)
8	BAT_THERM	0.1 to (VDDA - 0.1)	1	0.1 to (VDDA - 0.1)
9	BAT_ID	0.1 to (VDDA - 0.1)	1	0.1 to (VDDA - 0.1)
10	USBIN pin (over-voltage protected)[b]	4.35 to 6.5	1/4	1.09 to 1.63
11	Die-temperature monitor	0.4 to 0.9	1	0.4 to 0.9
12	0.625 V reference voltage	0.625	1	0.625
13	1.25 V reference voltage	1.25	1	1.25
14	–	–	–	–
15	Module power off[d]	–	–	–

a. Input voltage must not exceed internal VMAX voltage so as to prevent a forward-biased junction condition where correct module operation will cease. The VMAX voltage is defined as:

$$VMAX(x) = \max[vcoin(x), vbat(x), vchg(x), usb\_vbus(x)]$$

b. DCIN and USBIN are protected inputs, i.e., no voltage is applied to AMUX if the OVP FETs are off when either of the charging source is above the threshold.

c. Channels 6 and 7 are the expanded channels for MPP and ATEST measurements. The signal is taken from a 16-to-1 preMUX inside this module.

d. Set channel number to 15 when not in use so that the scaler does not load the inputs.

NOTE Gain and offset errors are different through each analog multiplexer channel. Each path should be calibrated individually over its valid gain and offset settings for best accuracy.

Performance specifications pertaining to the analog multiplexer and its associated circuits are listed in Table 19-2.

Table 19-2 Analog multiplexer performance specifications

Parameter	Comments	Min	Typ	Max	Units
Supply voltage		–	1.8	–	V
Output voltage range	Full specification compliance	0.100	–	1.70	V
	Degraded accuracy at edges	0.050	–	1.75	V
Input referred offset errors	Unity scaling				
Channel x1		-2	–	+2	mV
Channel x1/3[a]		-1.5	–	+1.5	mV
Channel x1/4		-3	–	+3	mV
Channel x1/6		-3	–	+3	mV

Table 19-2 Analog multiplexer performance specifications (Continued)

Parameter	Comments	Min	Typ	Max	Units
Gain errors	Includes scaler; excludes VREF error				
Channel x1		0.2	–	+0.2	%
Channel x1/3		0.15	–	+0.15	%
Channel x1/4		-0.3	–	+0.3	%
Channel x1/6		-0.3	–	+0.3	%
Integrated non-linearity	INL, after removing offset/gain errors	-3	–	+3	mV
Input resistance	Input referred to account for scaling				
Channel x1		10	–	–	MΩ
Channel x1/3		1	–	–	MΩ
Channel x1/4		0.5	–	–	MΩ
Channel x1/6		0.5	–	–	MΩ
Channel-to-channel isolation	f = 1 kHz	50	–	–	dB
Output settling time[b]	C_{load} = 65 pF	–	–	25	µs
Output noise level	f = 1 kHz	–	–	2	µV/Hz$^{1/2}$

a. Including process and temperature variations.

b. See Figure 19-2 for a model of the typical load circuit. C1 represents parasitic capacitance (0 to 20 pF); C2 is the sampling capacitor (63 pF); and S1 is the sampling switch (1 kW maximum). After S1 closes, the voltage across C2 settles within the specified settling time.

c. Multiplexer offset error, gain error, and INL are measured as illustrated in Figure 19-1. Supporting comments:

- The non-linearity curve is exaggerated for illustrative purposes.
- Input and output voltages must stay within the ranges stated in Table 19-2; voltages beyond these ranges result in non-linearity, and are beyond specification.
- Offset is determined by measuring the slope of the endpoint line (m), and calculating its Y-intercept value (b):
- Offset = b = y1 - m·x1
- Gain error is calculated from the ideal response and the endpoint line as the ratio of their two slopes (in percentage):

  Gain_error = [(slope of endpoint line)/(slope of ideal response) - 1]·100%
- INL is the worst-case deviation from the endpoint line. The endpoint line removes the gain and offset errors to isolate nonlinearity:

  INL(min) = min[Vout(actual at Vx input) - Vout(endpoint line at Vx input)]

  INL(max) = max[Vout(actual at Vx input) - Vout(endpoint line at Vx input)]

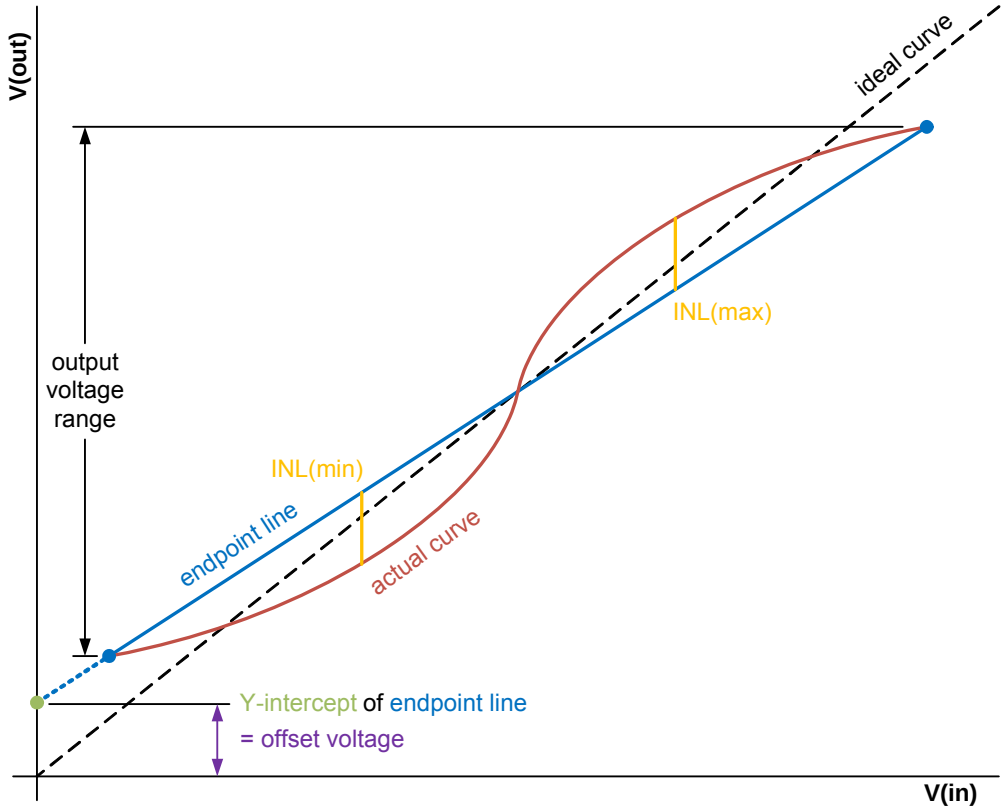

Figure 19-1 Multiplexer offset and gain errors

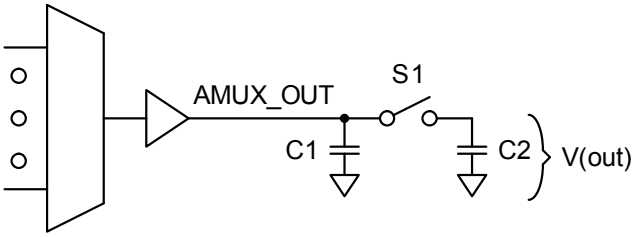

Figure 19-2 Analog multiplexer load condition for settling time specification

19.2.1 HK/XO ADC circuit

The PM8921 IC includes an analog-to-digital converter circuit that is shared by the housekeeping (HK) and 19.2 MHz crystal oscillator (XO) functions. A 2:1 analog multiplexer selects which source is applied to the ADC:

- The HK source – the analog multiplexer output discussed in Section 19.2; or
- The XO source – the thermistor network output that estimates the 19.2 MHz crystal temperature.

HK/XO ADC performance specifications are listed in Table 19-3.

Table 19-3 HK/XO ADC performance specifications

Parameter	Comments	Min	Typ	Max	Units
Supply voltage		–	1.8	–	V
Resolution		–	–	15	bits
Analog input bandwidth		–	100	–	kHz
Sample rate	XO/8	–	2.4	–	MHz
Offset error		-1	–	+1	%
Gain error		-1	–	+1	%
INL	15 bit output	-8	–	+8	LSB
DNL	15 bit output	-4	–	+4	LSB

AMUX input to ADC output end-to-end accuracy specifications are listed in Table 19-4.

Table 19-4 AMUX input to ADC output end-to-end accuracy specifications

AMUX ch #	Function	Typical input range		Auto scaling	Typical output range		AMUX input to ADC output end-to-end accuracy, RSS (%)[a,b]				AMUX input to ADC output end-to-end accuracy, WCS (%)[a,c]				Recommended method of calibration for the channel[d]
							Without calibration		Internal calibration		Without calibration		Internal calibration		
		Min (V)	Max (V)		Min (V)	Max (V)	Accuracy corresponding to min input voltage (V)	Accuracy corresponding to max input voltage (V)	Accuracy corresponding to min input voltage (V)	Accuracy corresponding to max input voltage (V)	Accuracy corresponding to min input voltage (V)	Accuracy corresponding to max input voltage (V)	Accuracy corresponding to min input voltage (V)	Accuracy corresponding to max input voltage (V)	
0	VCOIN	2	3.25	1/3	0.67	1.08	3.1	2.2	0.7	0.52	5.7	4.37	1.4	1.08	Absolute
1	VBAT	2.5	4.5	1/3	0.83	1.5	2.64	1.89	0.6	0.47	5	3.76	1.24	0.93	Absolute
2	OVP_SNS (protected)	4.5	9.5	1/6	0.75	1.58	2.84	1.84	0.62		5.33	3.68	1.31	0.92	Absolute
3	NC	–	–	–	–	–	–	–	–	–	–	–	–	–	–
4	VPH_PWR	2.5	4.5	1/3	0.83	1.5	2.64	1.89	0.6	0.47	5	3.76	1.24	0.93	Absolute
5	IBAT: battery charge current	0.3	1.5	1	0.3	1.5	6.3	1.87	1.33	0.47	10	3.73	2.33	0.93	Absolute
6	Selected input from pre-mux	0.1	1.7	1	0.1	1.7	18	1.76	4	0.47	26	3.59	6	0.88	Absolute or ratiometric, depending on application
7	Selected input from pre-mux	0.3	5.1	1/3	0.1	1.7	18.33	1.78	3.67	0.45	25.67	3.59	6.33	0.9	Absolute or ratiometric, depending on application
8	BATT_THERM	0.1	1.7	1	0.1	1.7	18	1.76	4	0.47	26	3.59	6	0.88	Ratiometric
9	BATT_ID	0.1	1.7	1	0.1	1.7	18	1.76	4	0.47	26	3.59	6	0.88	Ratiometric
10	USB_IN (protected)	4.35	6.5	1/4	1.09	1.63	2.21	1.82	0.53	0.46	4.34	3.68	1.08	0.88	Absolute
11	Die-temperature monitor	0.4	0.9	1	0.4	0.9	4.75	2.4	1	1.22	8	4.7	2	1.22	Absolute
12	0.625 V reference voltage	–	–	1	–	–	–	–	–	–	–	–	–	–	–
13	1.25 V reference voltage	–	–	1	–	–	–	–	–	–	–	–	–	–	–
14	NC	–	–	–	–	–	–	–	–	–	–	–	–	–	–
15	Poweroff	–	–	–	–	–	–	–	–	–	–	–	–	–	–

a. The min and max accuracy values correspond to min and max input voltage to the AMUX channel.

b. Accuracy is based on the root sum square (RSS) of the individual errors.

c. Accuracy is based on the worst-case sum (WCS) of all errors.

d. Absolute calibration uses the 0.625 V and 1.25 V MBG voltage reference as calibration points. Ratiometric calibration uses the GND_XO and VREF_XO_THM as the calibration points.

20 Voice Codec

20.1 Audio CODEC

The WCD9311 IC is a standalone audio codec IC that supports multimedia solutions, including the APQ8064 chipset. Key WCD9311 functions include:

- Serial low-power inter-chip media bus (SLIMbus) for access to on-chip digital audio channels with fewer pins relative to inter-IC sound (I2S) bus
- Seven analog input ports and eight analog output ports
- Seven analog-to-digital converters (ADCs) and eight digital-to-analog converters (DACs)
- Six digital microphone inputs (three clock/data pairs)
- Sidetone sample rate converter and infinite impulse response (IIR) filters for better performance and lower latency

The WCD9311 IC supports two I/O operating modes: SLIMbus and I^2S (selected using a dedicated hardware mode control pin). SLIMbus is the primary mode that provides access to all the audio codec paths and features, while I^2S provides access to fewer paths but maintains compatibility with earlier generation ICs.

This highly integrated IC is very small – it uses the 3.77 × 3.2 × 0.62 mm, 71 pin wafer-level nano-scale package (71 WLNSP) 6.0 × 6.0 × 1.27 mm, 86 pin chip-scale package (86 CSP) – and is supplemented by modem IC processing (such as the APQ8064 IC) to create an audio solution that reduces part count and PCB area. Companion chipsets ensure hardware and software compatibility to simplify the design cycle and reduce OEM time-to-market.

The WCD9311 IC uses low-power 65 nm CMOS fabrication technology, making it perfectly suited for battery-operated devices where power consumption and performance are critical.

20.1.1 Tx processing features

- Seven analog MIC input ports – six support differential and single-ended configurations, and one supports single-ended-only for the multibutton headset control (MBHC) feature
- Seven ADCs, one for each analog input
- MBHC with dedicated input to the ADC
  - Insertion/removal detection
  - Impedance (mic presence detection)
  - Detection for up to eight buttons
- Six digital microphone inputs with three clock lines, one for every digital microphone (DMIC) pair

- Ten concurrent Tx paths in SLIMbus mode
- 100 dB signal-to-noise ratio (SNR) (minimum) with 2.2 V analog supply and 0 dB gain mode
- SLIMbus interface that supports resolutions of 12, 16, 20, and 24 bits
- Input programmable gain settings of 0, 6, 12, and 18 dB
- Capless inputs (direct DC-coupled microphone support) and legacy capacitor-coupled inputs support
- Fixed input impedance of 10 k per pin (independent of amplifier gain) in input capacitor-coupled mode
- Four microphone bias circuits that can be used to power analog and DMICs
- Three independent pulse-code modulation (PCM) rates to support voice, music, and ultrasonic rates concurrently
- ANC path that is selectable from any ADC or digital microphone
- Digital gain control from -80 to +40 dB in 0.5 dB increments, plus mute
- Digital DC blocking filter with a selectable corner frequency of 3, 75, or 150 Hz
- Sample rates of 8, 16, 32, 48, 96, and 192 kHz
- 2 mW stereo record at 48 kHz sample rate

20.1.2 Rx processing features

- Eight analog outputs – earpiece, headphone left and right, and five line outputs
- Dynamic range enhancement (DRE) for HPH and line-out power amplifiers (PAs)
- Eight DACs and seven interpolation paths (earpiece and headphone-left share one DAC path)
- Seven concurrent Rx paths
- 110 dB (typical) headphone SNR
- SLIMbus interface that supports resolutions of 12, 16, 20, and 24 bits in isochronous mode
- Differential earpiece output
  - Class G, 125 mW into 32 W
- Stereo single-ended headphone outputs (16 or 32 W)
  - Capless, class G, 63 mW into 16 W (each)
- Five single-ended line outputs (600 W)
  - Four can be used as stereo differential
- Adjustable headphone and line output gain settings
- Auxiliary programmable gain amplifier (PGA) to DAC PA mixing on all analog outputs, plus stereo to mono mixing
- Digital mixing at the input of each DAC path
- Three independent PCM rates to support voice, music, and ultrasonic rates concurrently

- 4 mW stereo playback at a 48 kHz sample rate
- Sample rates of 8, 16, 32, 48, 96, and 192 kHz
- Over-current protection on headphone and earpiece outputs
- Click and pop suppression
  - -80 dBVpp A-weighted (maximum) on the headphone outputs
  - -60 dBVpp A-weighted (maximum) on earpiece and line outputs

20.1.3 Additional processing and paths

- ANC supports feedforward, feedback, and adaptive modes
- Two sidetone paths with processing
  - All mixed channels operate at the same sample rate
  - No gain changes occur as a result of mixing channels
  - Two five-stage IIR filters
  - Two sample-rate converters
- Two auxiliary PGAs
  - Connected to inputs 5 and 6
  - Mixing with all DAC paths
  - Independent gain (-42 to +12 dB in 1.5 dB steps) with zero-crossing detection

20.1.4 Support features

- DC power management
  - LDO generates 1.95, 2.35, 2.75, and 2.85 V for internal microphone bias circuits
  - Charge pump generates plus and minus voltages
  - Supply gating and distribution to all other blocks
- Clock circuits
  - Master clocks supported: 24.576, 19.2, 12.288, and 9.6 MHz
  - Clock buffering, gating, and distribution to all other blocks
- Digital data, status, and control
  - Dedicated over-current protection interrupt
  - SLIMbus
    - 2-line bus that supports seven Rx inputs and ten Tx outputs, plus framer
    - Input and output mixing with flexible selection of routing signal paths

- Inter-integrated circuit (I2C) provides the legacy control interface
  - Fast-speed (400 kbps) mode
- Integrated IEC electrostatic discharge (ESD) (8 kV contact)

20.1.5 Package and other features

- Small package – 3.77 × 3.2 × 0.62 mm, 71 WLNSP, 0.4 mm pitch 6 × 6 × 1.27 mm, 86 CSP, 0.5 mm pitch
- Many ground pins for improved electrical grounding, mechanical strength, and thermal continuity
- 65 nm CMOS technology
- Few external components required
- Pb-free, BrCl-free, RoHS compliant, SAC405 compliant

21 JTAG

The JTAG interface to the APQ8064 chipset provides debug, factory test, and board-level test support independent of the system logic. It provides for control and observation of both the boundary scan register and other scan registers used for device programming, security, and debug. The JTAG interface conforms to the ANSI/IEEE 1149.1 - 2001 and IEEE 1149.6 - 2003.

The chip has a primary JTAG interface on dedicated pins and an auxiliary interface (AUX JTAG) behind GPIOs. Both JTAG ports can be simultaneously run in various modes to allow simultaneous debug of ARM9, Krait, and ARM7 processors.

22 GPS/GNSS

Position location and navigation systems are supported through the RF IC's global navigation satellite system (GNSS) receiver using the WGR7640 IC. The APQ8064 chipset supports Gen8A (GPS and GLONASS) operation.

GPS features

- Next generation gpsOne solution with enhanced GPS engine and low-power tracking
- Enhanced navigation 3.0, dynamic power optimization, on-demand positioning, and SBAS (such as WAAS, EGNOS, MSAS)
- Support for Wi-Fi positioning
- MS/UE-based, MS/UE-assisted, hybrid modes with AFLT (CDMA) and MRL (UMTS), standalone and network-aware modes
- gpsOneXTRA Assistance for enhanced standalone GPS performance
- Control plane: IS-801, IS-881, and UMTS CP assisted-GPS protocols
- User plane: v1/v2 trusted mode and OMA SUPL 1.0 assisted-GPS protocols
- Wideband processing of GPS signals helps resolve multipath interference, promoting improved measurement accuracy

23 Camera

The APQ8064 supports a primary camera, webcam, and 3D camera capability.

Key camera features include:

- Primary (via 4-lane MIPI_CSI) – supports CMOS and CCD sensors
  - Up to 20 MP in-line JPEG encode at 15 fps
  - 60 fps WXGA viewfinder frame rate
  - A wide variety of pixel manipulation, camera modes, image effects, and post-processing techniques are supported, including defective pixel correction.
  - VFE raw dump of CSI data at line rate (4 Gbps) to PCDDR3
  - SMIA++ support
  - Plus inter-integrated circuit (I2C) or SPI control
- Secondary (via 2-lane MIPI_CSI) – provides webcam functions
  - Up to 8 MP
- 3D camera (via 1-lane MIPI_CSI)
  - Up to 8 MP
- In-line JPEG processing
  - No external RAM requirement for image snapshot processing
  - Reduced shot-to-shot latency for multishot photos

23.1 Image processing details

- MIPI camera serial interface (CSI)
  - 4-lane for primary camera
  - 2-lane for secondary camera such as web cam
  - 2-lane for 3D camera
- Camera operation data flow examples
- Video front-end (VFE)
- In-line JPEG
- HD codec

- Video pre-processing engine (VPE)
- Image processing examples

NOTE Parallel camera interface is not supported.

23.2 Video front-end (VFE)

VFE is the common interface between camera sensors and a variety of image and video compression standards (MPEG-4, H.263, and others).

Key VFE features include:

- Dedicated hardware blocks – like true DSC
- PCLK up 228 MHz in normal mode and 266 MHz in high clock mode
- Improves a DSP bandwidth and performance by offloading video processing tasks
- Entire image processing pipeline implemented with dedicated hardware blocks
- High programmability improves image quality and performance
- High-resolution, flexible image statistics for accurate and robust AWB/AE/AF
- AWB/color conversion statistics are collected and used to control VFE blocks
- AE/AF statistics for sensor compensation through I2C
- Multiple simultaneous outputs
- Image sensor inputs are routed directly to external memory for bandwidth-efficient off-line processing

23.3 In-line JPEG

The in-line JPEG encoder reduces latency, useful as a frame-based encoder for encoding rotated pictures and for frame-based processing.

23.4 Video preprocessing engine (VPE)

Provides processing in real-time before encoding, including:

- Digital image stabilization
- Digital zoom
- Rotation
- Overlay

23.5 HD video codec

The HD video codec can encode or decode multiple 30 fps image streams of up to 1080p resolution (1920 x 1080). The support standards include:

- ITU-T H.264, ISO/IEC 14496-10
- ITU-T H.263
- ISO/IEC 14496-2 MPEG4 and DivX®
- ISO/IEC 13818-2 MPEG2
- SMPTE 421M VC-1

23.6 Example image processing capabilities

Table 23-1 Viewfinder/video mode

Parameter	Capability
Maximum viewfinder resolution	1080p
Maximum viewfinder refresh rate	30 fps
Max viewfinder / video output resolution	1080p
Comprehensive scaling and cropping	1080p
Viewfinder ASF	5x5
3A	Version 2.2
50/60 Hz beating	Auto flicker detect and correct
Lens roll-off correction	Mesh-based
Memory color enhancement	Viewfinder-based / WYSIWYG with snapshot
Real-time histogram	Y, RGB
Special effects	Sepia, B/W, solarization, etc.

Table 23-2 Snapshot / JPEG Mode

Parameter	Capability
Maximum snapshot resolution	20 MP
Maximum input data rate	4096 Mbps 4-lane CSI 2048 Mbps 2-lane CSI
Simultaneous snapshot + 1080p encode	Yes
JPEG processing latency	TBD (to be provided in a future revision of this document)
Flash	Xenon and white LED
Mechanical shutter	Not supported
GPS capability via OEM application	Insert GPS lat/long into JPEG EXIF header
JPEG file control	By file size, by quality

24 Graphics

Graphic features include:

- Adreno 320™ graphics core
  - Supports high end dual displays (1080p + WQXGA)
  - Fully programmable unified shader architecture rendering
    - GPGPU shader program
  - Better pixel performance
    - Support for higher resolutions
    - Double pixel/texel throughput
    - Faster resolve rate
  - Dedicated on-chip memory for graphics
  - Better 2D Performance
- 2D/3D graphics acceleration:
  - Adreno 320 graphics: 200 M peak triangles/sec; 6.4 B vector shader instructions/sec; 3.2 BP/sec; 3.2 B texel/sec
  - APIs include OpenGL ES 1.x, 2.0, and 3.0; Direct3D Dx9.x; C2D for 2D composition; OpenCL for Adreno 320
- Adreno 320 hardware acceleration of Web and UI applications:
  - Flash applications and fonts accelerated with native OpenCL 1.1 hardware
  - 2D bitmap elements rendered concurrent with 3D rendering
  - 2D rendered elements can be texture mapped to 3D UI concurrently

Table 24-1 Graphic specifications

Parameter	Capability
Clock	400 MHz / 325 MHz (turbo / nominal)
Peak vector shader instruction rate	6400M instructions per second
Peak 3D triangle rate	200M triangles per second
Peak 3D pixel draw rate	3200M pixels per second
2D pixel draw rate concurrent w/ peak 3D	TBD pixels per second
Combined 2D + 3D pixel draw rate	TBD pixels per second

Table 24-1 Graphic specifications

Parameter	Capability
Primary LCD max resolution	WSXGA
Dedicated hardware for 2D	Yes
APIs provided	OpenGLES 1.x, 2.0, 3.0 Direct3D Dx9.0 w/ Shader model 2.0 HLSL Direct3D Dx9.3 w/ Shader model 3.0+ HLSL OpenCL 1.1 embedded profile (for GPGPU) C2D (for 2D composition)

25 MIPI Support

The APQ8064 device supports the MIPI CSI and MIPI DSI interfaces.

25.1 MIPI camera serial interfaces

- MIPI CSI
  - Two MIPI CSI interfaces
    - 2-lane and 4-lane for dual camera support
  - Per Mobile Industry Processor Interface (MIPI) specification
  - One high-speed clock lane and one to four data lanes
  - Low-voltage differential signaling (LVDS)
  - PHY block provides physical interface to camera sensor

25.2 MIPI display serial interfaces

- MIPI DSI
  - Two MIPI DSI interfaces
    - 3-lane and 4-lane for dual display support
  - Per Mobile Industry Processor Interface (MIPI) specification
  - One high-speed clock lane and one to four data lanes
  - Low-voltage differential signaling (LVDS)
  - PHY block provides physical interface to display device

25.3 3D camera

The APQ8064 device supports a third MIPI camera serial interface (CSI2, 1-lane). This approach enables support for not only the primary camera and the webcam, but adds support for a 3D camera (using CSI0 and CSI1 plus webcam using CSI2).

26 HDMI Support

The APQ8064 high-definition multimedia interface (HDMI) transmitter drives television sets, projectors, etc.

26.1 HDMI features

- HDMI Rev. 1.4a (w/HDCP)
- Integrated HDMI Tx core and HDMI PHY
- 1080p at 60 Hz refresh; 24-bit RGB color
- Up to 8-channel audio for 7.1 surround sound
- Dolby Digital Plus, Dolby True-HD, and DTS-HD Master
- Supported specifications: HDMI version 1.3b and HDCP system version 1.3
- Video pixel encoding: RGB444
- Video color depth: 24 bpp
- Video formats per CEA-861-D: 640 × 480p, 1280 × 720p, 1920 × 1080i, 720 × 480p, 720 (1440) × 480i, all at 60 Hz; 1280 × 720p, 1920 × 1080i, 720 × 576p, 720(1440) × 576i, all at 50 Hz; and 1280 × 720p, 1920 × 1080p at 24, 25, 30, 50, and 60 Hz
- Audio channels supported: 2 (L, R; 2 channel L-PCM) and 8 (7.1 surround sound; 8 channel L-PCM 24-bit /192 kHz)
- Audio sample rates: 32, 44.1, 48, 88.2, 96, 144, 176.4, and 192 kHz

26.2 MI^{2}S for HDMI 7.1 surround sound

Table 26-1 Surround sound

Parameter	Performance	Comments
I^{2}S master or slave	Both	
Sample rates	8, 16, 24, 32, 48, 96 kHz	
Clock rates	64·Fs, 128·Fs, 256·Fs	Audio playback example: MCLK is typically 256·48 kHz = 12.228 MHz
Channel support	Stereo	
Resolution	16, 24, 32 bits	
Duplex support	Full duplex	

27 WSXGA support

Using the MDP display core, the APQ8064 provides 24-bit WSXGA (1440 x 900) display support.

More information to be provided in a future revision of this document.

28 Wireless Connectivity

WLAN and Bluetooth functionality is controlled by the QCA6234 device.

28.1 QCA6234 overview

28.1.1 General description

The QCA6234 is a complete, small form factor 2x2 802.11 a/b/g/n WLAN plus BT4.0 combo solution optimized for low-power, mobile consumer electronic devices. The device integrates all WLAN and BT functionality in a single package to support a low cost, layout-friendly implementation while allowing flexibility for platform specific customization.

The QCA6234 integrates the complete transmit/receive RF paths including baluns, switches, and reference oscillator. The device is also pre-calibrated, eliminating the need for customer production calibration.

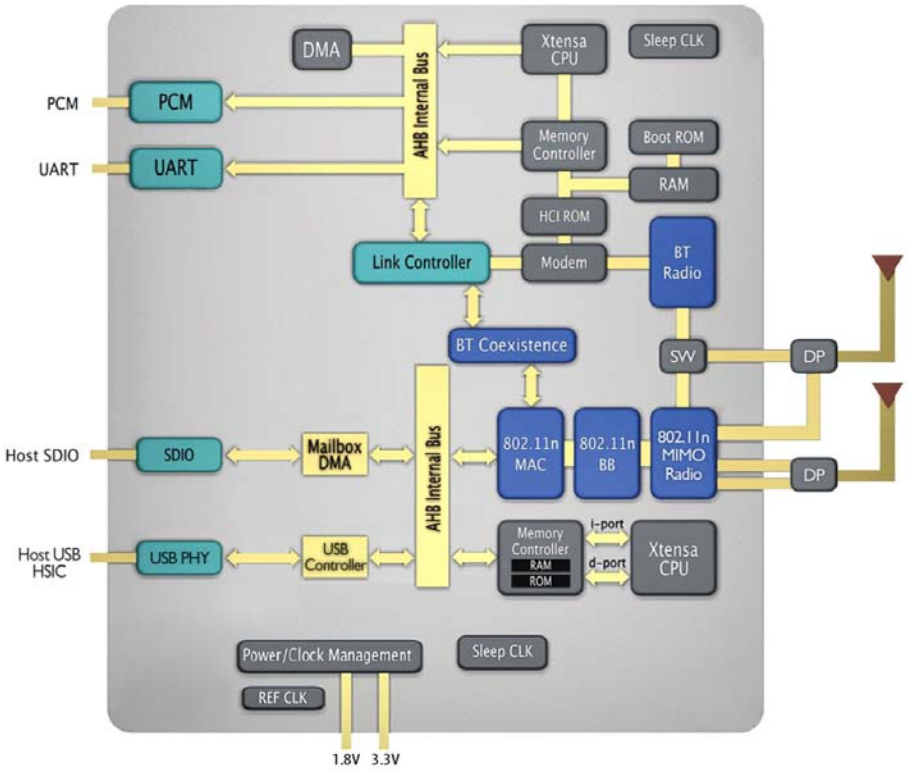

Figure 28-1 AR6234 system block diagram

QCA6234 supports Bluetooth 2.1 + EDR and Bluetooth low energy (Bluetooth 4.0) standards enabling seamless integration of BT/WLAN and Low Energy technology. A flexible BT RAM/ROM split architecture enables optional customization to meet customer specific needs and use cases. Ultra low power consumption radio architecture and proprietary power save technologies extend battery life. Embedded on-chip CPUs handle complete 11n and BT MAC/BB/PHY processing to minimize host processor loading.

QCA6234 is available in 4 variants:

- QCA6234X: 2x2, dual-band 802.11n and Bluetooth 4.0
- QCA6234G: 2x2, single-band 802.11n and Bluetooth 4.0
- QCA6204X: 2x2, dual-band 802.11n
- QCA6204G: 2x2, single-band 802.11n

QCA6234G/X is pin compatible with QCA6204G/X standalone 802.11n solution, enabling designers with flexibility to address different application requirements with either a combo or standalone 11n solution, while maintaining the same PCB design.

See Table 28-1 for QCA6234/QCA6204 options.

Table 28-1 QCA6234/QCA6204 options

Part No.	2.4 GHz	5 GHz	BT 2.1/4.0
QCA6234X	x	x	X
QCA6234G	x		X
QCA6204X	x	x	
QCA6204G	x		

QCA6234 is available in a low profile 9.2 mm × 9.2 mm LGA package with 0.65 mm pitch pads for low-cost PCB design. It is halogen-free, Pb-free and fully ROHS compliant.

28.1.2 QCA6234 features

- Two stream (2x2) 802.11n provides highest throughput and superior RF performance for hand-held devices
- Advanced 2x2 802.11n features:
  - 40MHz channels at 5 GHz
  - Half Guard Interval for high throughput
  - Frame Aggregation for high throughput
  - Space Time Block Coding (STBC) Rx for improved downlink robustness over range
  - Low Density Parity Check (LDPC) encoding for improved uplink and downlink robustness over range
  - Maximum Ratio Combining (MRC)
  - Transmit Beamforming (TxBF)
  - Maximum Likelihood (ML) Decoder

- Supports popular interfaces used in embedded designs:
  - SDIO 2.0 (50 MHz, 4-bit and 1-bit) for WLAN;
  - High-speed UART (up to 4 Mbps).
- Bluetooth low energy (BT4.0) ready.
  - Class 1.5 Bluetooth with integrated Tx/Rx switch.
- All WLAN RF transmitters are pre-calibrated
- Near zero power consumption in idle and stand-by enables users to leave WLAN and BT "always on."
- Advanced BT/WLAN coexistence and concurrent RX for superior rate-over-range and very low latency.
- Best in class Rx sensitivity for superior throughput rate-over-range performance
- Integrated Sleep Clock eliminates the need for expensive bulky 32 KHz real-time clock.
- Integrated conformal RF shielding and near-zero RBOM for lowest cost.
- Supports RTT (round trip time) based ranging measurement to any Wi-Fi devices for indoor positioning.

28.2 QCA6234 features summary

28.2.1 Overview

The QCA6234 is a single package combination IEEE 802.11 a/b/g/n plus Bluetooth 4.0 device based on cutting edge technology from the AR6004 ROCm family of mobile 11n and AR3002 ROCm family of HCI-ROM Bluetooth devices. The QCA6234 contains dual 802.11 and Bluetooth radios, including full digital MAC and baseband engines handling all 802.11 CCK/OFDM® 2.4 GHz, and Bluetooth basic rate and EDR baseband and protocol processing. Dual embedded low-power CPU cores minimize host loading and maximize flexibility to support customer specific profiles and use cases.

The QCA6234 is available in 4 variants: QCA6234X, QCA6234G, QCA6204X and QCA6204G. QCA6234G/X is a small form factor 802.11n plus Bluetooth 4.0 combo; QCA6204G/X is a standalone 802.11n solution.

The QCA6234G/X is pin compatible with the QCA6204G/X, enabling designers with flexibility to address different application requirements with either a combo or standalone 11n solution, while maintaining the same PCB design.

28.2.2 Radio front end

The QCA6234 integrates the complete transmit/receive RF paths including baluns, switches, and reference oscillator. External diplexers are required for dual-band WLAN implementation.

28.2.3 Industry leading coexistence

Qualcomm Atheros, Inc. proprietary WLAN/BT coexistence algorithms, proven in millions of handset and portable devices shipped-to-date, enable superior rate-over-range throughput and low-latency performance in harsh real-world operating conditions.

The algorithms optimize important use cases such as (just to list a few) Bluetooth mono voice audio (HSP/HFP), Bluetooth stereo audio (A2DP) and Bluetooth data transfer profiles (OPP, FTP, etc.) in parallel with WLAN traffic including concurrent operation of BT2.1+EDR and BT-LE cases.

The use cases are optimized to provide the highest WLAN throughput, long range and low power consumption while maintaining the best Bluetooth audio quality, high data throughput, and low-latency. The highly flexible hardware and software architecture of the QCA6234 enables simple and rapid deployment of customization and enhancements of the coexistence algorithm to support any future use cases.

28.2.4 Power management

QCA6134 can run on one 3.3 volt power supply and an I/O supply of 1.8V or 3.3V. Both WLAN and Bluetooth power management utilize advanced power saving techniques such as:

- Gating clocks to idle or inactive blocks
- Voltage scaling to specific blocks in certain states
- Fast start and settling circuits to reduce Tx
- Active duty cycles
- CPU frequency scaling
- Other techniques to optimize power consumption across all operating states

28.2.5 Manufacturing calibration

The QCA6234 is fully RF system tested and calibrated in production, simplifying the radio testing on the customer production line and eliminating the need for calibration.

28.2.6 Reference frequency

The QCA6234 incorporates a 26 MHz reference frequency source in package. Internally, the system reference frequency is sleep regulated and gated to enable the internal crystal to be powered down when the device is in sleep mode. Manufacturing calibration of the crystal is not required.

28.2.7 Internal sleep clock

The QCA6234 incorporates integrated on-chip low power sleep clocks to regulate internal timing, eliminating the need for any external 32 KHz real time clocks or crystal oscillators.

28.2.8 Interfaces

The QCA6234 supports industry standard WLAN and Bluetooth host interfaces:

- SDIO 2.0 (50 MHz, 4-bit and 1-bit) for WLAN
- HS-UART for Bluetooth HCI (Host Controller Interface) and is compatible with any upper layer Bluetooth stack.

28.2.9 Mobile 802.11n

The QCA6234 incorporates the latest generation of mobile 802.11n technology from Qualcomm Atheros, Inc. The QCA6234 is 802.11n compliant and features:

- Half Guard Interval for high throughput.
- Frame Aggregation for high throughput.
- Space Time Block Coding (STBC) Rx for improved downlink robustness over range.
- Low Density Parity Check (LDPC) for improved uplink and downlink robustness over range.

Table 28-2 lists the 802.11n (PHY layer) throughput at different modulations.

Table 28-2 802.11n (PHY layer) throughput at different modulations

Mode	MCS	Modulation	Data Rate (Mbps) 20 MHz Channel	
			FGI[a]	SGI[b]
IEEE 802.11n	0	BPSK	6.5	7.2
	1	QPSK	13.0	14.4
	2	QPSK	19.5	21.7
	3	16-QAM	26.0	29.9
	4	16-QAM	39.0	43.3
	5	64-QAM	52.0	57.8
	6	64-QAM	58.5	65.0
	7	64-QAM	65.0	72.2
	8	BPSK	13.0	14.4
	9	QPSK	26.0	28.9
	10	QPSK	39.0	43.3
	11	16-QAM	52.0	57.8
	12	16-QAM	78.0	86.7
	13	64-QAM	104.0	115.6
	14	64-QAM	117.0	130.0
	15	64-QAM	130.0	144.4

a. Full guard interval = 800 ns
b. Short guard interval = 400 ns

28.2.10 Advanced WLAN features

The QCA6234 is fully compliant with IEEE 802.11e QoS, WiFi Alliance WMM Power Save and 802.11n power saving, ensuring the lowest possible power consumption.

Advanced features such as Host wake-on-wireless and ARP (address resolution protocol) off-loading enable the WLAN link to remain associated for extended periods with host processor asleep for additional deep system power savings.

The QCA6234 features hardware-based AES, AES-CCMP, and TKIP engines for faster data encryption, and supports industry leading security features including Cisco CCXv4 ASD, WAPI (for China), WLAN Protected Setup (WPS), along with standard WEP/WPA/WPA2 for personal and enterprise environments.

Other WLAN features include:

- WWR, 802.11d, 802.11h
- WLAN Protected Setup (WPS)
- Wi-Fi Direct
- RTT (Round Trip Time) for indoor locationing
- Device based scanning & roaming, tunable parameters optimized for seamless handover
- Statistics and events for monitoring
- Self-managed power state handling
- Self-contained beacon processing
- Shared authentication
- Ad-hoc power save
- Multiple PMK Id support
- Simulated UAPSD
- T-Spec support
- Production flow diagnostics
- Dynamic PS-Polling for enhanced coexistence performance with Bluetooth
- QoS support for VoIP applications
- Bluetooth 3.0 HS (High Speed) 802.11 AMP (Alternate MAC PHY)

28.2.11 AP mode (mobile hot spot)

Qualcomm Atheros' industry-leading AP Mode feature allows the QCA6234 device to operate as both a station and an Access Point, enabling seamless station-to-station interconnection with all the benefits of standard infrastructure-level simplicity (no special client software or settings required), security, and power save functionality. AP Mode enables the deployment of unique and powerful applications such as mobile 3G gateway and mobile range extension.

28.2.12 WiFi Direct (peer-to-peer)

Qualcomm Atheros' industry leading WiFi Direct implementation of advanced peer-to-peer connectivity enables faster device-to-device data and media transfer, improved network efficiency eliminating the *hop* through the access point, simultaneous connection to the device and the Internet, and simple PAN setup (with WLAN Protected Setup), all with reduced power consumption to extend battery life.

28.2.13 Host offloading (WLAN)

The QCA6234 integrates extensive hardware signal processing and an embedded on-chip CPU to offload complete 11n MAC/BB/PHY processing to minimize host processor loading and support application specific customization for gaming and mobile phones.

The QCA6234 offloads the complete 802.11 b/g/n baseband and MAC functions as standard feature, including:

- Link Maintenance
- 802.11 frame transmission sequence to initiate the connection with an Access Point;
- Background scanning, including transmission of Probe Request;
- Signal quality detection and automated maintenance of current Access Point list;
- Roaming to a new Access Point
- Rate Adaptation, including automatic retry
- Encapsulation of 802.3 frames from the host to 802.11 frames. This includes adding the security headers for 802.11
- Decapsulation of the 802.11 frame to 802.3 frame
- Encryption & decryption (hardware ciphers) for WEP/TKIP/AES-CCMP, and WAPI
- IEEE PowerSave. Periodic wakeup when in sleep mode to check for buffered traffic
- Packet Filtering and Host Wakeup, including ARP (Address Resolution Protocol) Response. Automated filtering of received data in the sleep mode to transfer only data packets of interest to the host.
- Frame Aggregation (A-MPDU) processing
- LDPC encode/decode and STBC decode
- Additionally, the QCA6234 also provides host offloading of the following advanced features:
  - TCP Checksum
  - Security negotiation: perform initial and subsequent 4-way handshake offload and initial Group Key exchange and Re-Keying

28.2.14 Advanced Bluetooth

QCA6234 incorporates an integrated low power Bluetooth radio, supporting all mandatory and optional features. Advanced architecture and protocol techniques, including DMA off-load, clock gating and clock scaling, hardware-based page/inquiry scan, enable very low power operation in all states and modes.

QCA6234, for Linux®-based OS, supports all standard profiles on BlueZ stack, including (but not limited to):

- GAP: Generic Access Profile
- SPP: Serial Port Profile
- HSP: Headset Profile
- HFP: Hands-Free Profile
- A2DP: Advanced Audio Distribution Profile
- AVRCP: Audio/Video Remote Control Profile
- FTP: File Transfer Profile
- PAN: Personal Area Networking Profile
- OPP: Object Push Profile
- HID: Human Interface Device Profile

The flexible RAM/ROM based architecture enables custom or future profiles to be easily added.

29 Exhibit 1

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